부산대 특강

반도체 산업 엿보기

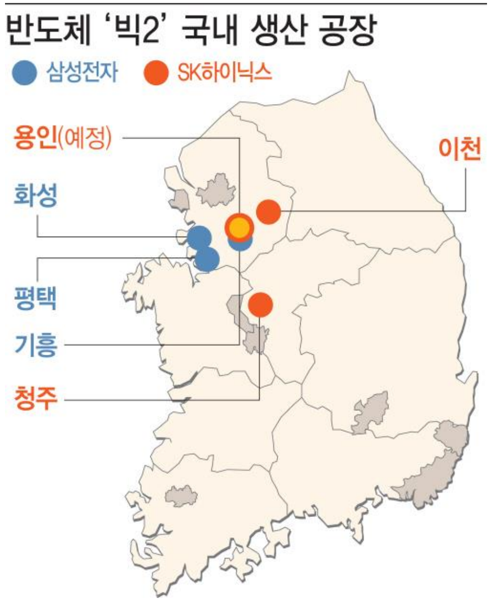
엄영제

FAB (Semiconductor Fabrication plant)

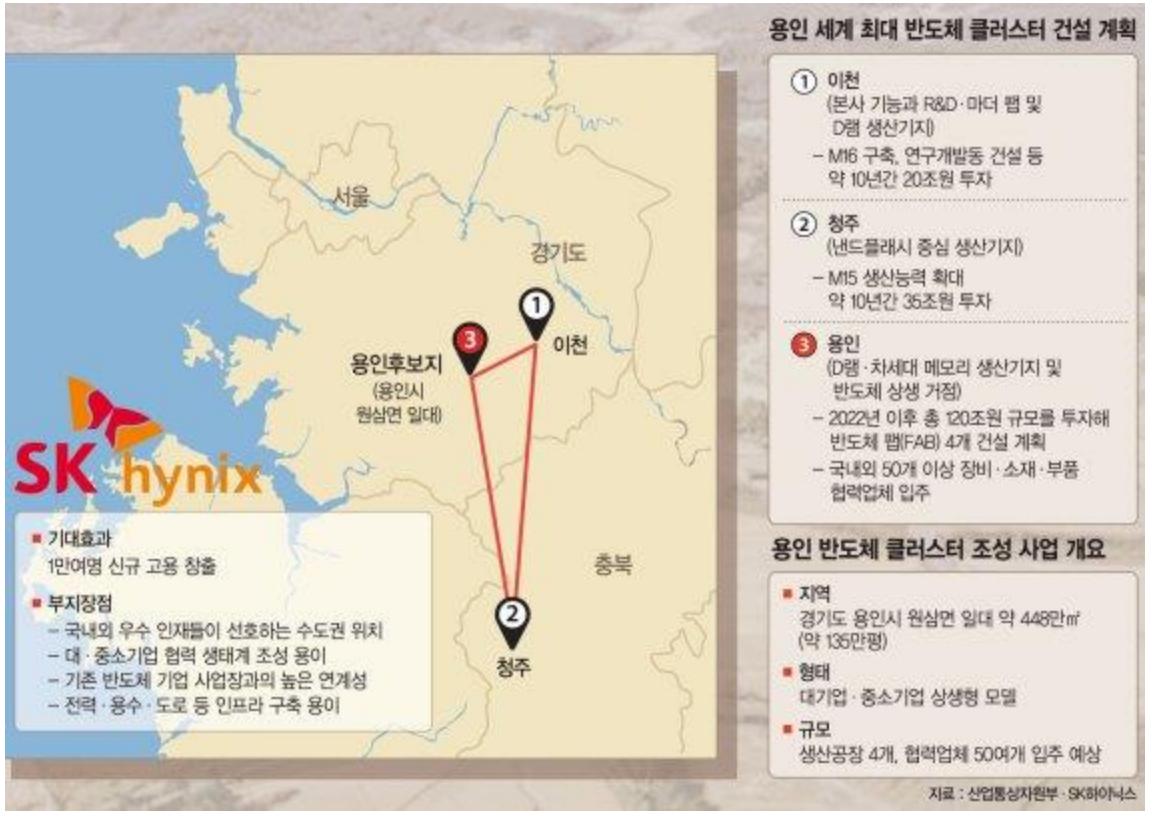
삼성 평택캠퍼스

FAB (Semiconductor Fabrication plant)


용인 반도체 클러스터 위치


반도체 ‘빅2’ 국내 생산 공장

● 삼성전자 ● SK하이닉스



- 기대효과
  1만여명 신규 고용 창출
- 부지장점
  - 국내외 우수 인재들이 선호하는 수도권 위치
  - 대·중소기업 협력 생태계 조성 용이
  - 기존 반도체 기업 사업장과의 높은 연계성
  - 전력·용수·도로 등 인프라 구축 용이

용인 세계 최대 반도체 클러스터 건설 계획

① 이천
(본사 기능과 R&D·마더 팹 및 D램 생산기지)
- M16 구축, 연구개발동 건설 등 약 10년간 20조원 투자

② 청주
(낸드플래시 중심 생산기지)
- M15 생산능력 확대 약 10년간 35조원 투자

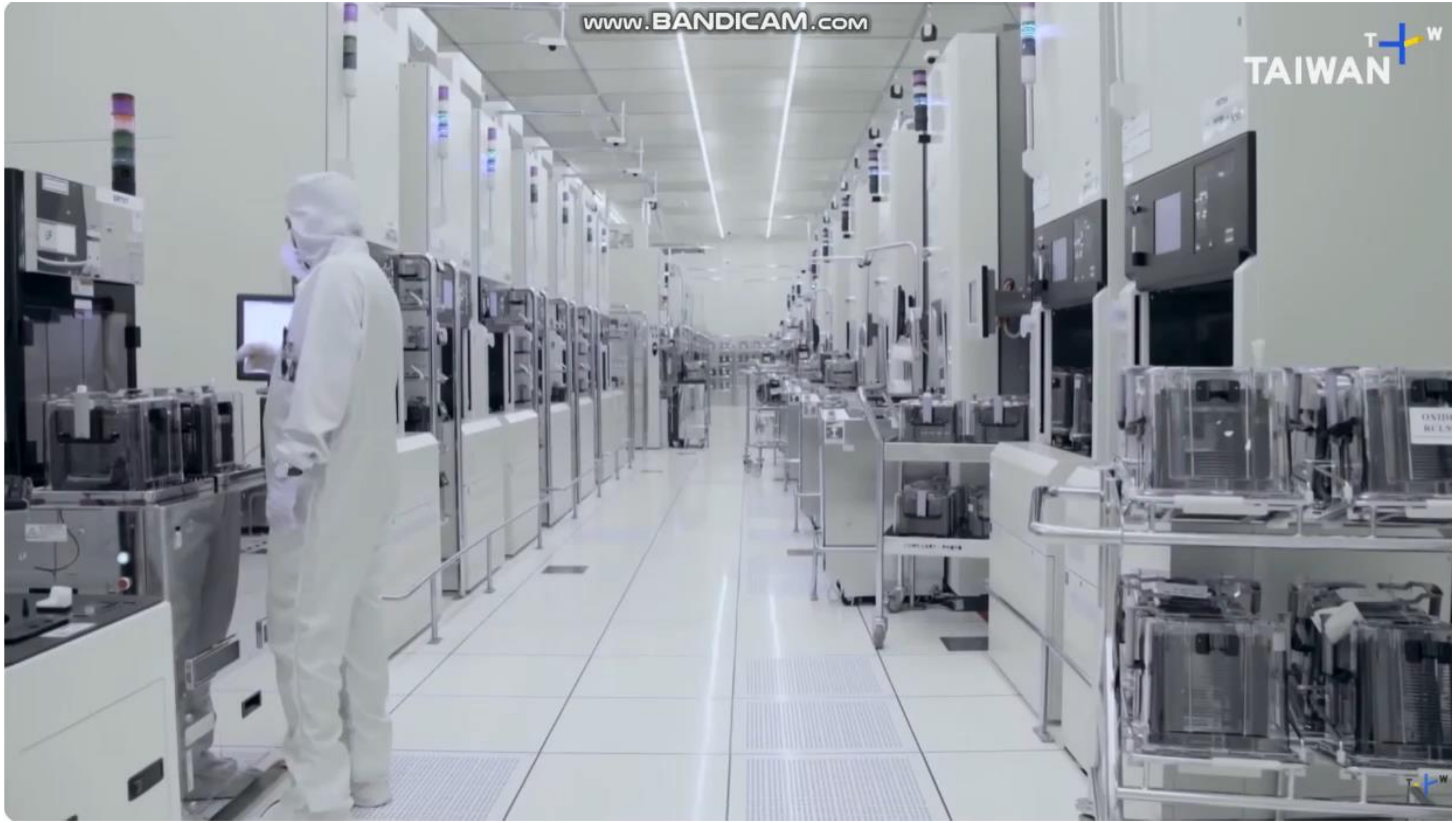
③ 용인
(D램·차세대 메모리 생산기지 및 반도체 상생 거점)
- 2022년 이후 총 120조원 규모를 투자해 반도체 팹(FAB) 4개 건설 계획
- 국내외 50개 이상 장비·소재·부품 협력업체 입주

용인 반도체 클러스터 조성 사업 개요

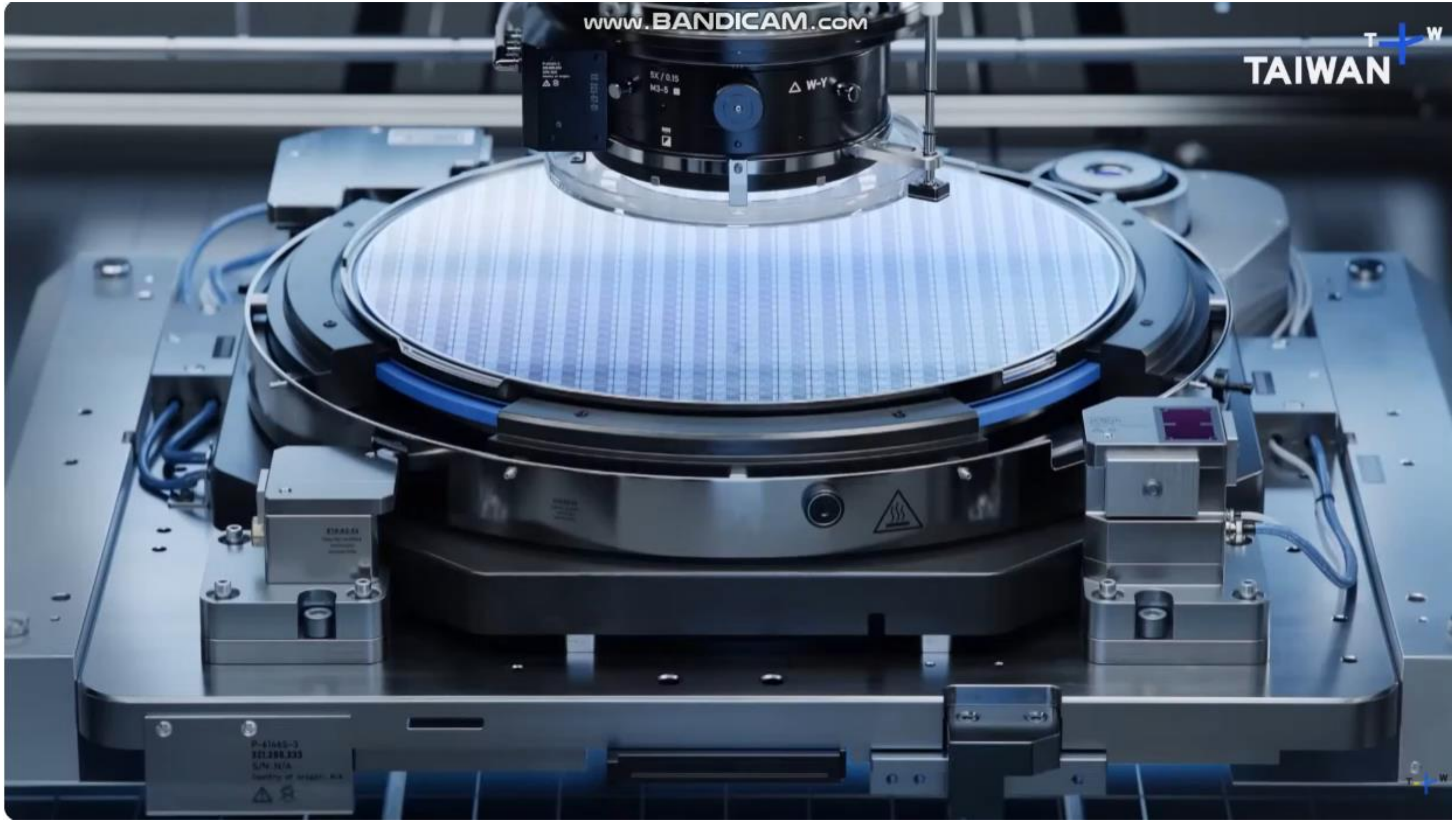
- 지역
  경기도 용인시 원삼면 일대 약 448만㎡ (약 135만평)
- 형태
  대기업·중소기업 상생형 모델
- 규모
  생산공장 4개, 협력업체 50여개 입주 예상

자료 : 산업통상자원부·SK하이닉스

FAB (Semiconductor Fabrication plant)



FAB (Semiconductor Fabrication plant)



SEMICON Korea 2026

February 11 – February 13, 2026
COEX, Seoul, Korea

Special

SAMSUNG SK hynix DB HiTek

Diamond

Lam RESEARCH TEL

Platinum

ADVANTEST APPLIED MATERIALS KLA

Gold

FUJIFILM PSK SEMES ASM Qnity Kashiyama KKTech
YC HANMI 한미반도체 WONIK IPS axcelis HITACHI KOKUSAI ELECTRIC
KSM SCREEN Innovation for a Sustainable World Lotvacuum MiCo Family

Silver

Air Liquide ASE CONPROFE DONGJIN SEMICHEM HORIBA KANKEN
BISTelligence Camtek Cohu DOOPLE FST FINE SEMITECH CORP. ISC
JSR NEXTIN NOVA onto innovation Park SYSTEMS PDF/SOLUTIONS
safeworld SUNGDO ENG SZU KOREA TERADYNE ThermoFisher SCIENTIFIC TSE
txOne networks UniTest UPChem

Intro I 반도체 산업 구조

서비스

NVIDIA
amazon
TESLA
Meta

소자

SAMSUNG
SK hynix
tsmc
Micron
intel

장비

APPLIED MATERIALS
ASML
Lam RESEARCH
KLA
TEL
SEMES

부품, 소재

soulbrain
DONGJIN
JSR
WONIK MATERIALS
MERCK
MiCo
HORIBA

Intro I 반도체 Workflow

Device & Process Design

Unit Process

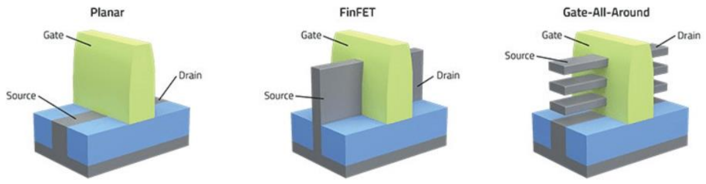
수율 및 불량 분석

Packaging

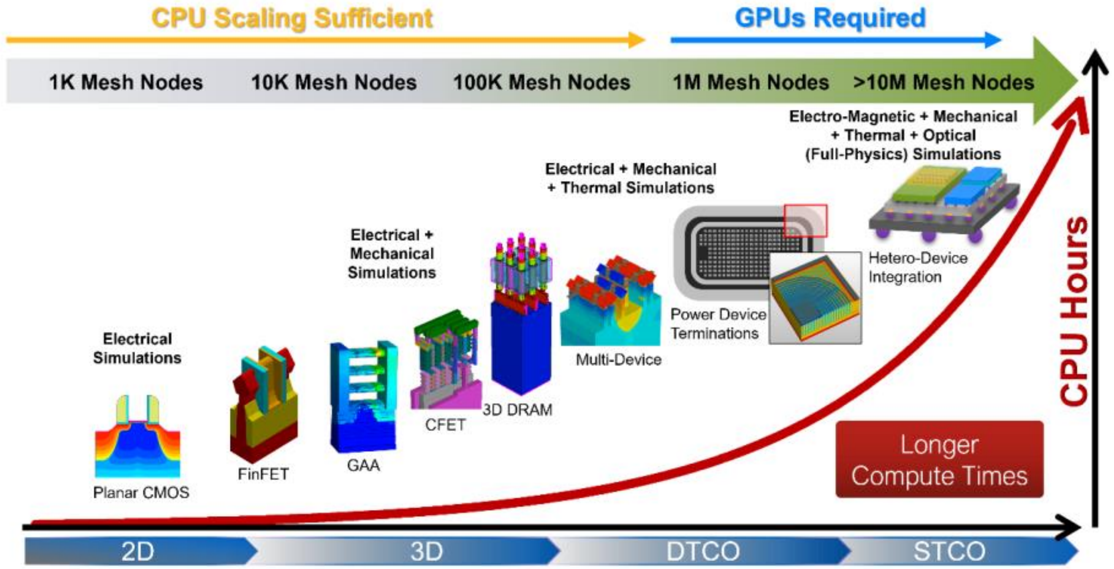
Intro | 반도체 Workflow

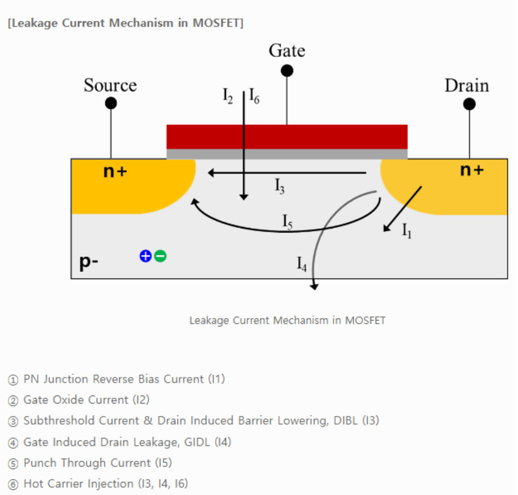
Device & Process Design → **Unit Process** → **수율 및 불량 분석** → **Packaging**

TD : Technology Development
PA : Process Architecture
PI : Process Integration



소자 구조 설계, 공정 시뮬레이션 (TCAD), 회로 설계 등

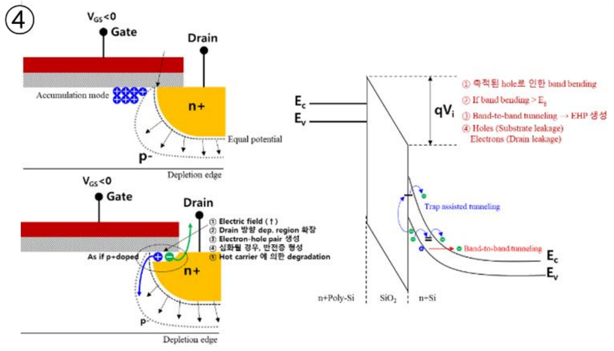




[Leakage Current Mechanism in MOSFET]

Leakage Current Mechanism in MOSFET

① PN Junction Reverse Bias Current (I1)
② Gate Oxide Current (I2)
③ Subthreshold Current & Drain Induced Barrier Lowering, DIBL (I3)
④ Gate Induced Drain Leakage, GIDL (I4)
⑤ Punch Through Current (I5)
⑥ Hot Carrier Injection (I3, I4, I6)

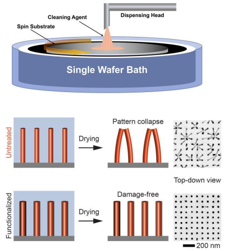
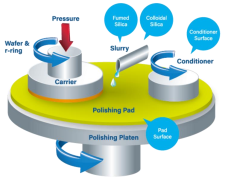
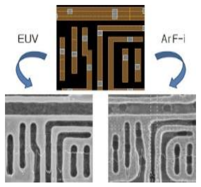
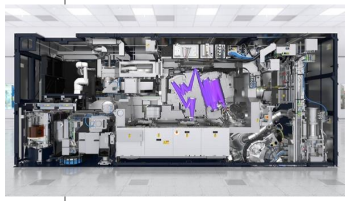
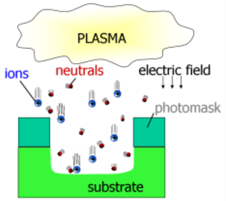
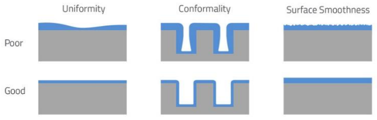
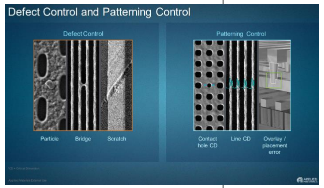


Intro | 반도체 Workflow

Device & Process Design → Unit Process → 수율 및 불량 분석 → Packaging

8대 공정 : Clean, CMP, Photo (Litho), Etch, Depo, Inspection & Metrology

준비 → 패턴 → 증착 → 검사

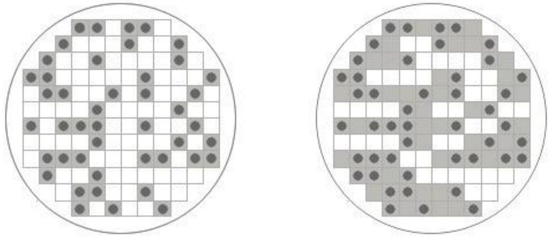
공정	세정 (Wet Clean)	평탄화 (CMP)	PR 도포/현상 (Spinner)	노광 (Photo-Litho)	식각 (Etch)	증착 (Depo)	검사
회사	SCREEN TEL	APPLIED MATERIALS	TEL	ASML	Lam RESEARCH APPLIED MATERIALS TEL	APPLIED MATERIALS	APPLIED MATERIALS KLA HITACHI Inspire the Next
기술	나노 파티클 제거, 초임계, 공학 (로봇 등)	Slurry, Warpage	Spin 코팅, 현상, 공학 (로봇 등)	KrF, ArF, EUV (파장), 분해능	Plasma Etch, ALE, Selective Etch	CVD, PECVD, ALD	광학, E-beam
							

Intro | 반도체 Workflow

Device & Process Design → **Unit Process** → **수율 및 불량 분석** → **Packaging**

YE : Yield Enhancement

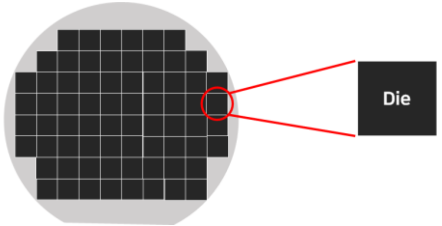
$$\frac{\text{실제 생산된 정상 칩 수}}{\text{설계된 최대 칩 수}} \times 100 = \text{수율(Yield)}$$

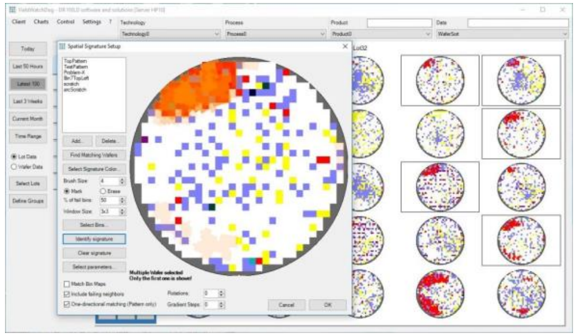


(a) 약 60% 수율 (a) 약 30% 수율

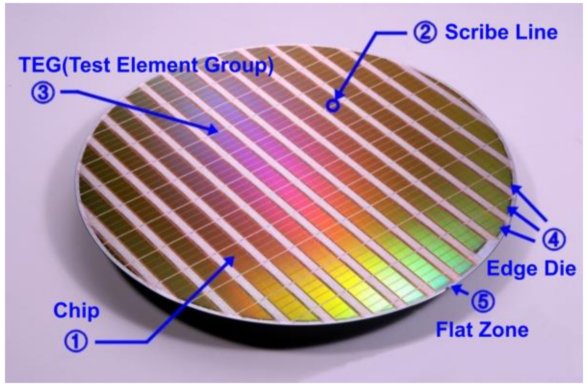
삼성반도체이야기
samsungsemiconstory.com

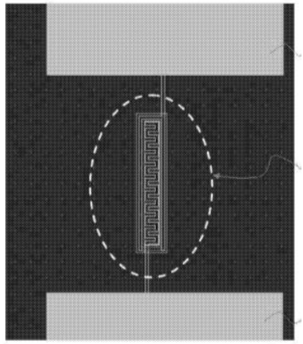
ET (Electrical Test)
EDS(Electrical Die Sorting)



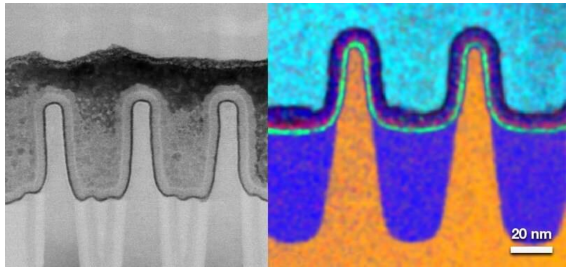


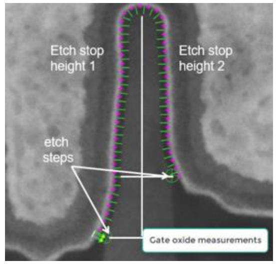
TEG (Test Elements Group)





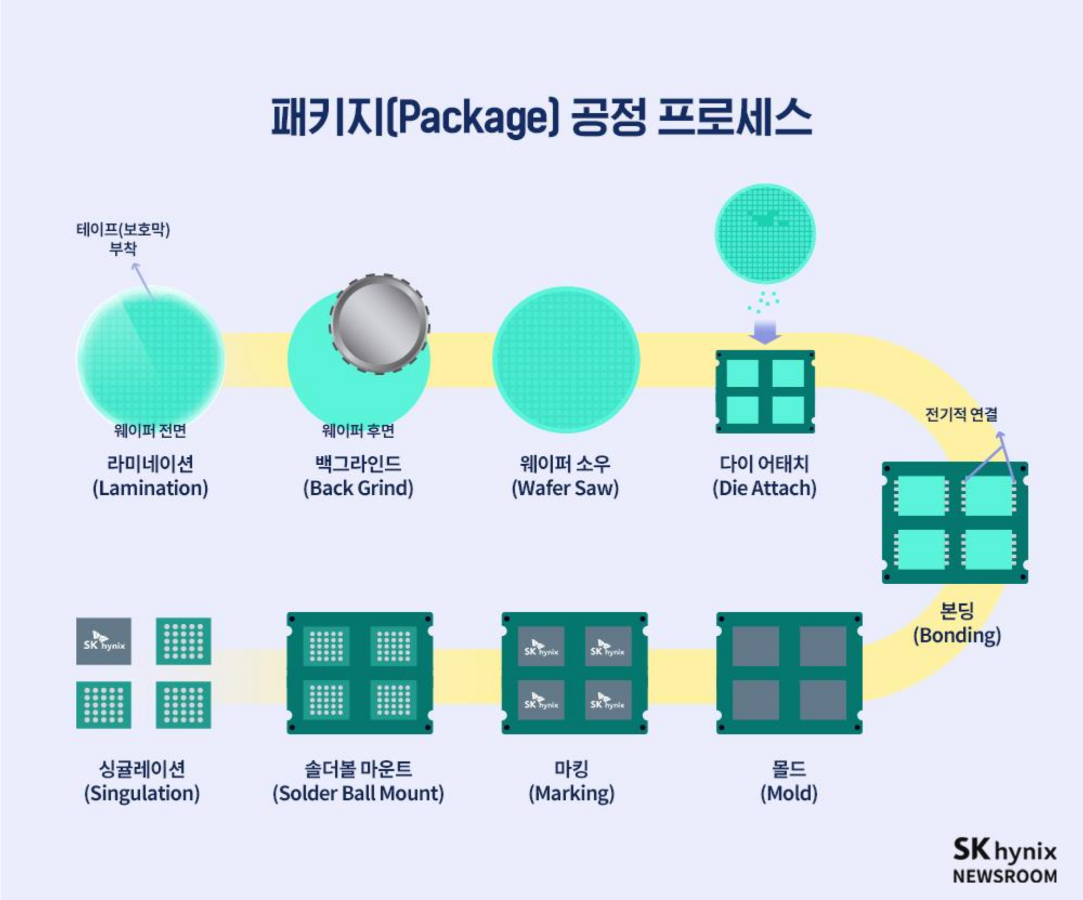
FA : Failure Analysis (TEM)





Intro | 반도체 Workflow

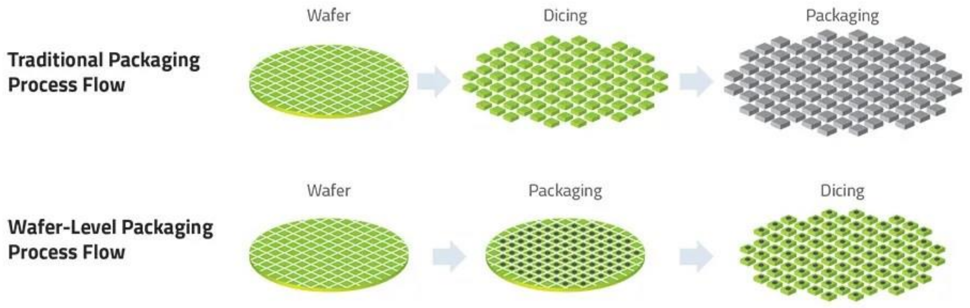
Device & Process Design → Unit Process → 수율 및 불량 분석 → **Packaging**

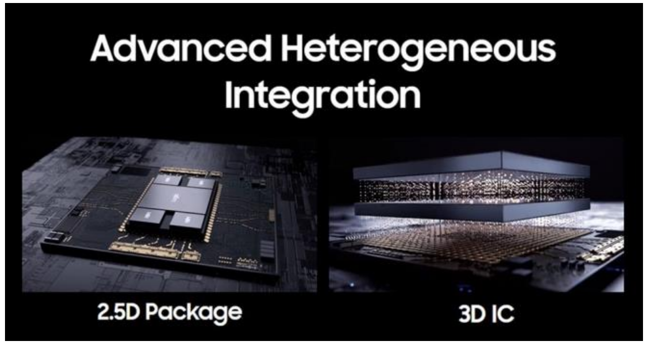


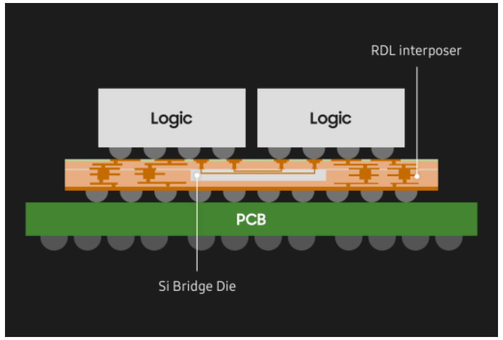
기존

OSAT(Outsourced Semiconductor Assembly and Test)

Advanced Packaging



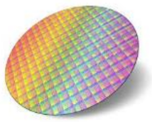




반도체
Device

반도체 | 반도체

서비스



소자

장비

부품, 소재

국민일보 | 6시간 전 | 네이버뉴스

'삼성 60%, TSMC 55%' 3나노 수율 역전... 삼성 파운드리 '탈환' ...

삼성전자는 TSMC를 제치고 주요 고객을 확보했던 '경험'이 있다. **삼성**전자는 2015년 TSMC보다 먼저 14나노 공정 진입에 성공했고 애플, 퀄컴 등의 물량을 대부분...

삼성 파운드리, 3나노 수율 TSMC 역전 성공... 엔비디아·... 에이빙뉴스 | 27분 전

뉴스1 PiCK | 1일 전 | 네이버뉴스

"우리가 1위""거기 문제 많아"...삼성·SK 얼굴 붉히게 한 차세대 반...

그러면서 "현재 엔비디아(GPU)와 TSMC(파운드리), SK하이닉스(HBM) 등 각 분야에서 시장을 리드하는 업체 간 협업을 더 중요시한다"고 덧붙였다. **삼성**전자는 ...

위기가 기회, 연간 10조 적자 전망에도 선명해진 K칩 '초... 메트로신문 | 1일 전

"삼성·마이크론보다 기술상 우위"...SK하이... 헤럴드경제 | 1일 전 | 네이버뉴스

서울경제 | 13면 9단 | 22시간 전 | 네이버뉴스

TSMC, 고급 칩 결합 분야 약진 "패키징 매출 53억弗...30% 껑충"

한편 TSMC의 파운드리 라이벌인 **삼성**전자는 프리스마크가 집계한 후공정 회사 톱15에 오르지 못했다. 패키징 설비를 갖춘 온양·천안 사업장에서는 주로 자체 메...

매일경제 PiCK | 20시간 전 | 네이버뉴스

"반도체 회복시점 이 때"...최태원 회장과 추경호 부총리가 콕 짚...

최태원 회장 "좀 더 버티면 연내 경기 반등한다" 그래도 장미빛 전망 **삼성**전자, SK하이닉스 등 국내 대표 기업들부터 TSMC와 인텔까지! 글로벌 산업의 핵심인 반...

에이빙뉴스 | 28분 전

삼성 파운드리, 3나노 수율 TSMC 역전 성공... 엔비디아·AMD·퀄...

생산 초기 수율 잡기에 난항이 따를 것을 우려해 TSMC와 인텔은 2nm부터 GAA를 도입할 예정이다. 반면 **삼성**전자는 앞서 GAA에 대한 노하우를 누적한 덕분에 생...

한국경제 PiCK | 3일 전 | 네이버뉴스

삼성도 못 만든 걸 만들겠다?...자신감 드러낸 日 기업 [정영효의 ...

그런데도 2030년대 초반에는 **삼성**전자와 TSMC도 아직 생산하지 못하는 1㎚급 최첨단 반도체를 양산하겠다고 발표했다. 2025년 2nm급 반도체 시제품을 생산한...

뉴스1 | 5일 전 | 네이버뉴스

"삼성 파운드리 4나노 수율 75%...퀄컴·엔비디아 고객 돌아올 것"

3nm 이하 파운드리 자체 난이도도 높기 때문에 이미 3nm GAA 수율이 60%이상 올라온 **삼성**전자가 2nm 경쟁해서도 유리하다는 분석이다. 여기에 TSMC의 평균...

디지털데일리 PiCK | 2023.06.26. | 네이버뉴스

[소부장 TF] ⑦ 美 칩스법 中 겨냥... 진퇴양난 삼성·SK

이중 첨단 반도체 기준은 28나노미터공정(nm) 미만의 로직 반도체와 18나노미터공정(nm) D램, 128단 이상의 낸드플래시가 해당된다. 이 기준이라면 **삼성**전자, S...

글로벌이코노믹 | 2023.06.29.

[초점] 美, 내달 對中 반도체 수출 통제 최종안 발표...삼성전자·SK...

상무부의 이번 최종안은 중국에 진출한 **삼성**전자와 SK**하이닉스** 등 한국의 반도체 기업에 직접적인 영향을... 낸드플래시는 **128단**으로 정의했으나, 한국 정부는 이 ...

ZDNet Korea PiCK | 4일 전 | 네이버뉴스

메모리 반도체장비 시장 '혹한'...삼성·SK 투자 감소 '직격타'

마이크론 등이 설비투자 규모를 지연 축소한 데 따른 영향으로 풀이된다. 13일 SEMI(국제**반도체**장비재료협... 지역별로는 **한국**, **중국**, 대만이 올해와 내년 장비 지...

연합뉴스 PiCK | 2023.07.07. | 네이버뉴스

"韓업체, 마이크론이 잃은 中반도체시장 대체금지 이행 어려워"

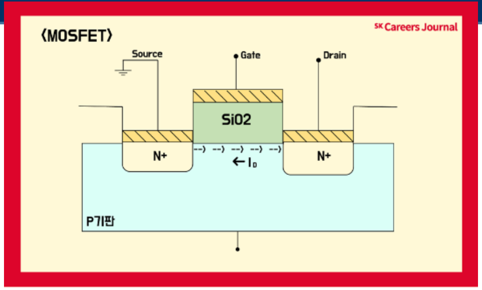
특파원 = **한국 반도체** 기업들이 **중국** 당국으로부터 판매 금지 조치를 당한 미국 **반도체**기업 **마이크론**의 시장 점유율을 채우지 않도록 금지하는 게 현실적으로 ...

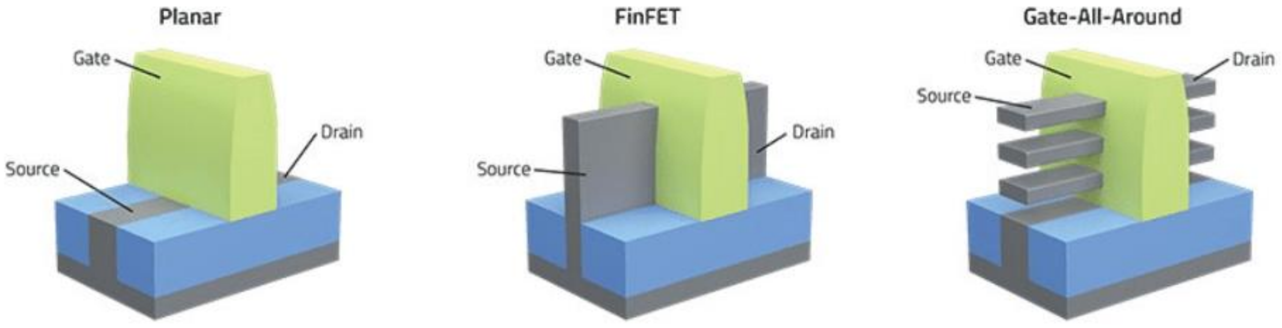
반도체 I 종류

소자 Type	계산 (Logic)	기억 (Memory)	
종류	**Logic (Foundary)**	**DRAM**	**NAND**
기능	계산	단기 기억	장기 기억
회사	**TSMC**, 삼성, 인텔	**삼성**, 하이닉스, 마이크론	**삼성**, 하이닉스, 마이크론
Keyword			

반도체 | 종류

소자 Type	계산 (Logic)
종류	**Logic (Foundary)**
기능	계산
회사	**TSMC**, 삼성, 인텔
Keyword	






국민일보 | 7시간 전 | 네이버뉴스

'삼성 60%, TSMC 55%' 3나노 수율 역전... 삼성 파운드리 '탈환' ...

인텔 파운드리를 활용할 가능성도 열어두고 있다"고 말했다. 삼성전자가 3나노부터 게이트올어라운드(GAA) 공정을 선제 도입한 점도 유리하게 작용할 것으로 보...

삼성전자 3나노 파운드리 수율 TSMC 앞지른 듯, ... 비즈니스포스트 | 12분 전

삼성 파운드리, 3나노 수율 TSMC 역전 성공... 엔비디... 에이빙뉴스 | 1시간 전

뉴시스 | 2일 전 | 네이버뉴스

[칩스토리]삼성전자 파운드리, TSMC 따라잡을 '히든카드'는?

삼성전자가 TSMC보다 먼저 GAA라는 새 공정을 도입하고도 수율 안정에 성공하며 파운드리 업계에 판도 변화 가능성이 높아진다. 미세공정 '마의 벽' 돌파구로 ...

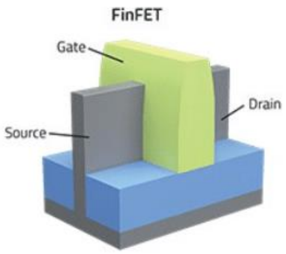
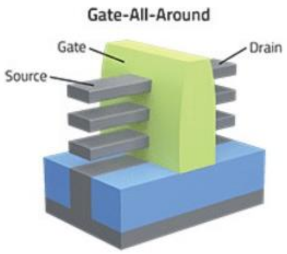
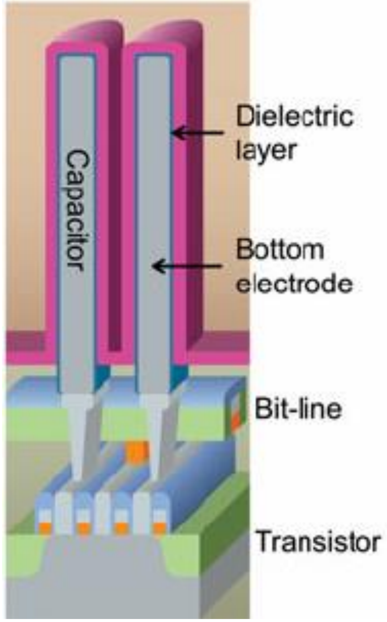
삼성전자 파운드리, TSMC 따라잡을 '히든카드'는? 글로벌이코노믹 | 2일 전

파이낸셜뉴스 PiCK | 5일 전 | 네이버뉴스

엔비디아·퀄컴 다시 돌아오나...삼성 4나노 수율 75%까지 올렸다

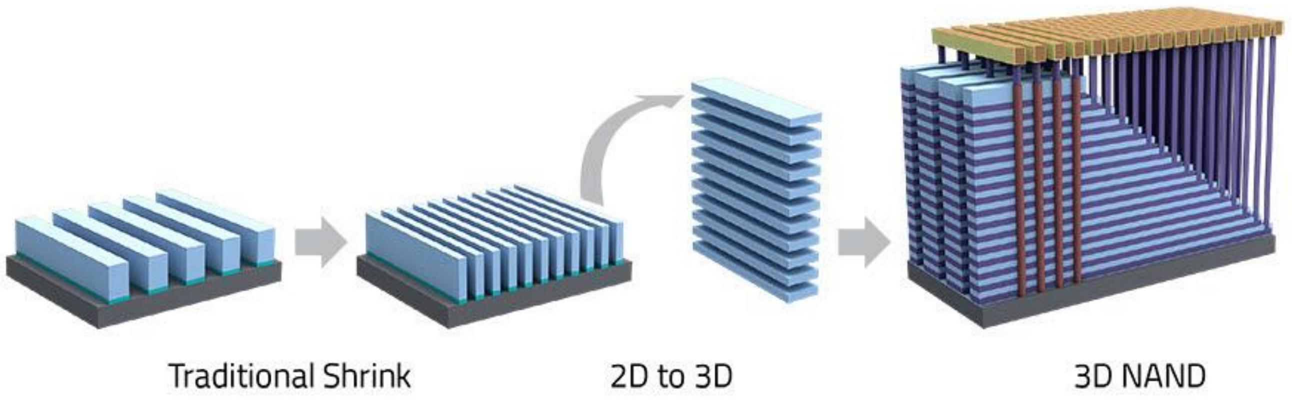
잡는데 어려움을 겪을 것으로 전망된다"며 "3나노 이하 파운드리 자체 난이도도 높기 때문에 이미 3나노 GAA 수율이 60%이상 올라온 삼성전자가 2나노 경쟁에서...

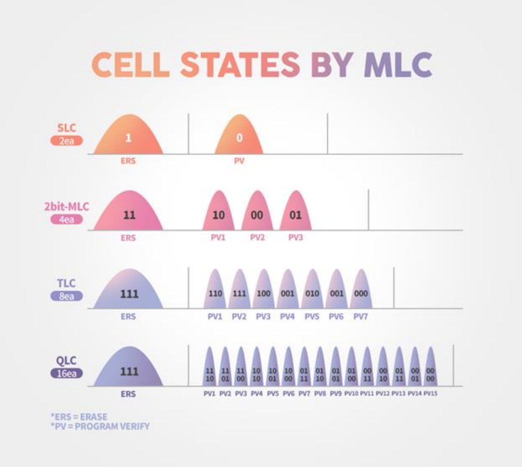
반도체 I 종류

소자 Type	계산 (Logic)	기억 (Memory)	
종류	**Logic (Foundary)**	**DRAM**	**NAND**
기능	계산	단기 기억	장기 기억
회사	**TSMC**, 삼성, 인텔	**삼성**, 하이닉스, 마이크론	**삼성**, 하이닉스, 마이크론
Keyword	**OO nm**, FinFET, GAA   	**Capacitor**, High-k (고유전율)  	

반도체 | 종류

소자 Type	기억 (Memory)
종류	**NAND**
기능	장기 기억
회사	**삼성**, 하이닉스, 마이크론
Keyword	





시사저널이코노미 2023.05.16.

SK하이닉스, **238단 낸드** 양산 앞두고 복잡해진 라인업 고민

메모리 반도체 업황은 지난해 하반기 이후 글로벌 경기침체에 따른 수요 급감으로 악화 추세다.... SK하이닉스가 **238단 낸드** 양산을 서두를 이유가 없단 견해도 있...

이투데이 2023.01.04.

[10대 경제 희망키워드 ③반도체 부활] 최고층 '**238단 낸드**' 성공...

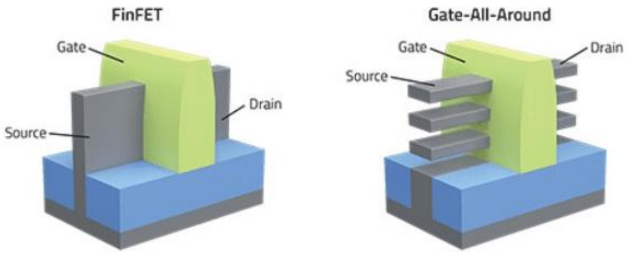
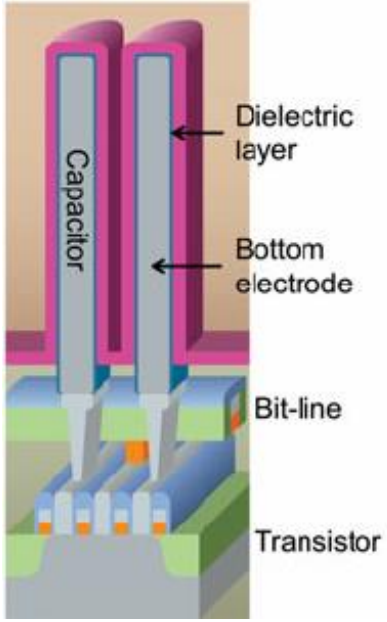
향후 수요 급증이 예상되는 차세대 전략 제품을 개발·출시해 미래 **메모리** 시장을 선도한다는 목표를 세웠다. 지난해 8월 SK하이닉스는 현존 세계 최고층인 '**238단**...

글로벌경제 2023.04.23.

中, 첨단반도체 '자력갱생' 추진... YMTC, 3D**낸드플래시** 생산 추진

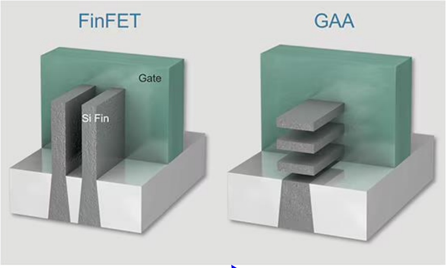
SK하이닉스가 지난해 8월 현존 최고층 **238단** 512기가비트(Gb) **TLC**(Triple Level Cell) 4D **낸드플래시** 개발에... **낸드플래시**는 전원이 꺼져도 데이터가 저장되는 **메모**...

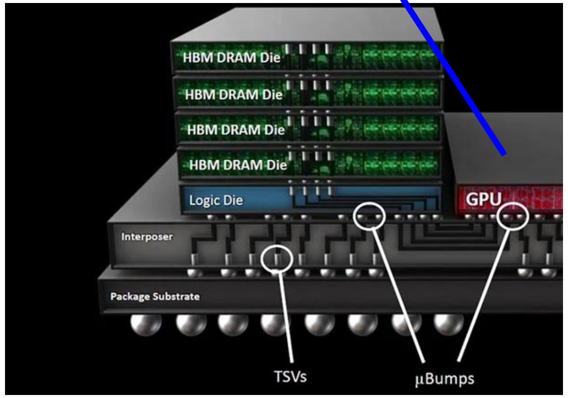
반도체 I 종류

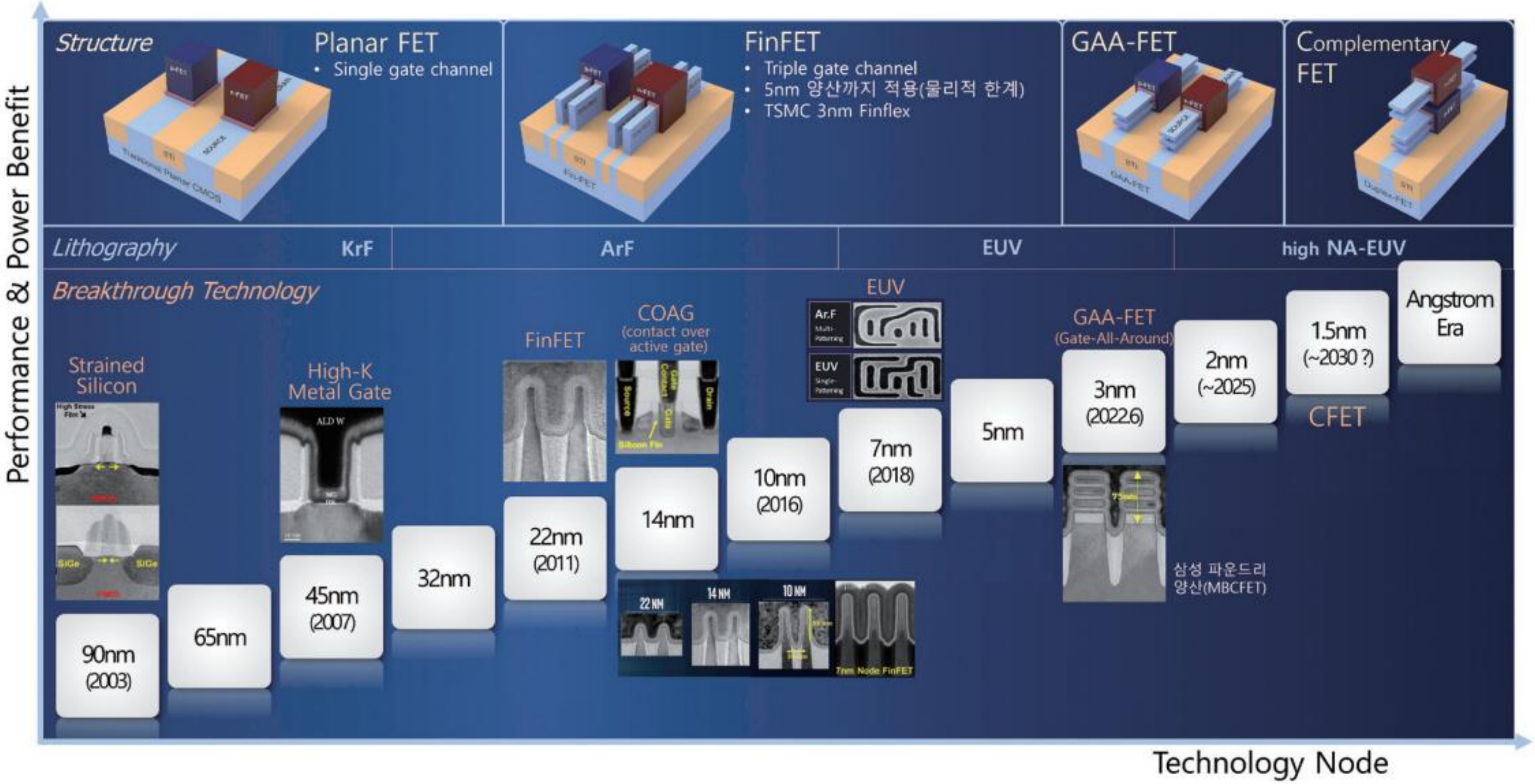
소자 Type	계산 (Logic)	기억 (Memory)	
종류	**Logic (Foundary)**	**DRAM**	**NAND**
기능	계산	단기 기억	장기 기억
회사	**TSMC**, 삼성, 인텔	**삼성**, 하이닉스, 마이크론	**삼성**, 하이닉스, 마이크론
Keyword	**OO nm**, FinFET, GAA  	**Capacitor**, High-k (고유전율)  	**OO 단** 

반도체 I Logic

Logic

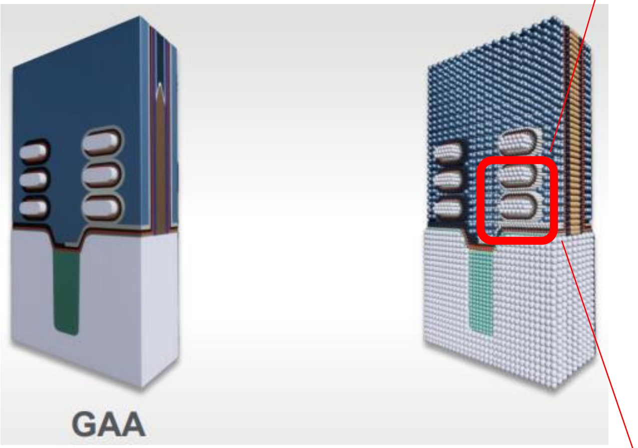


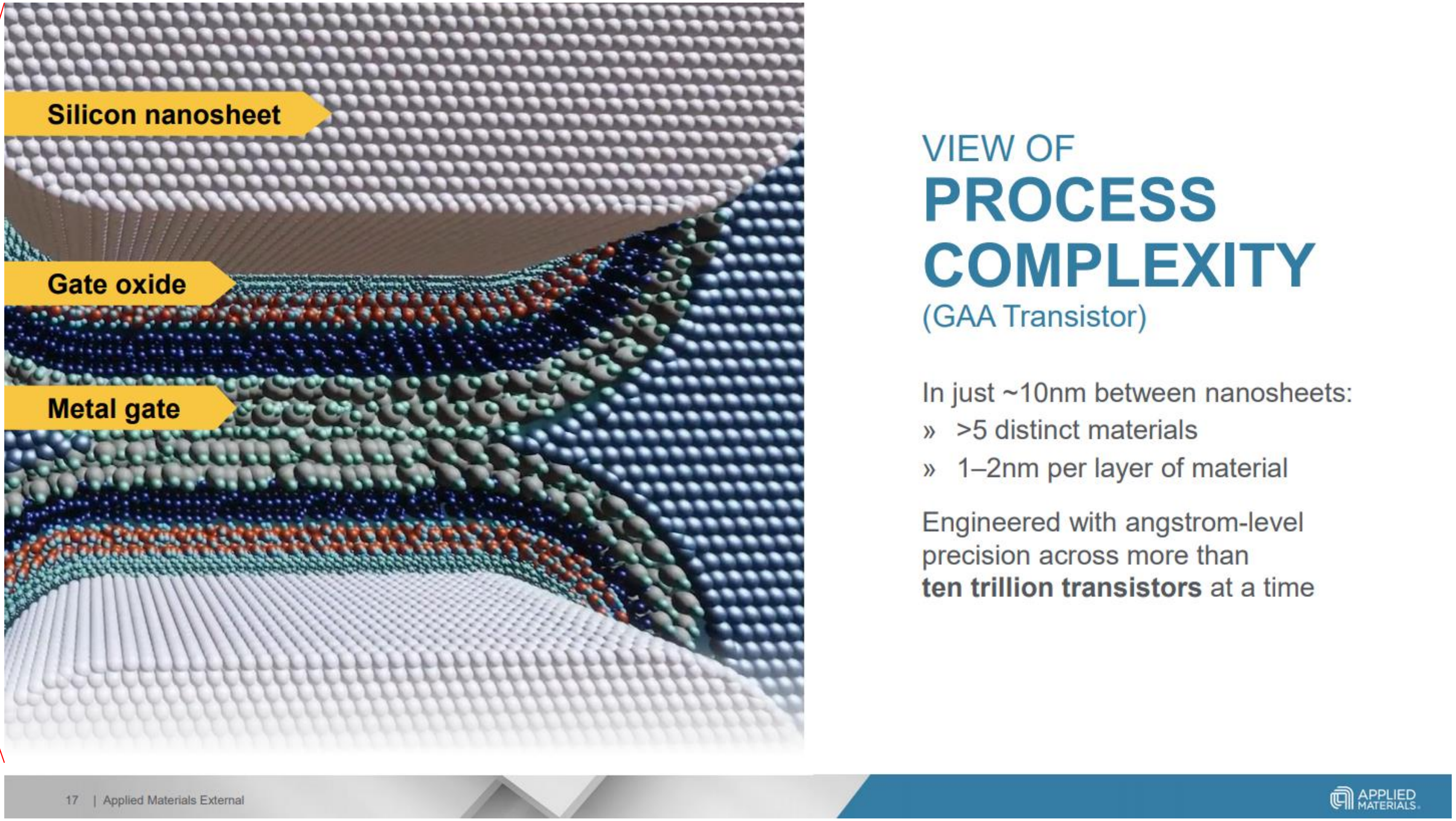




https://ettrends.etri.re.kr/ettrends/205/0905205006/0905205006.html

반도체 | Logic





VIEW OF

PROCESS COMPLEXITY

(GAA Transistor)

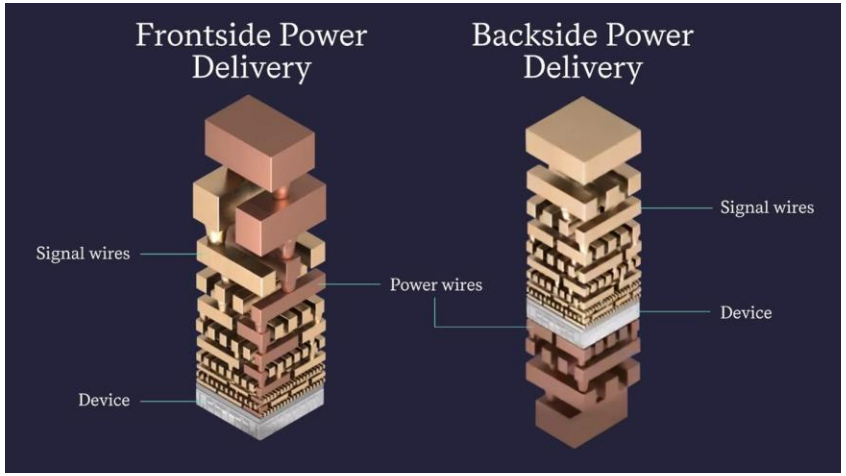
In just ~10nm between nanosheets:

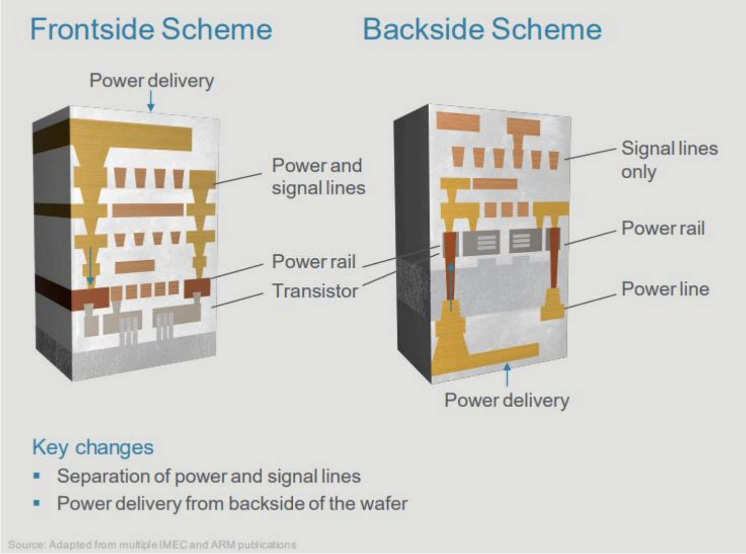
- >5 distinct materials
- 1–2nm per layer of material

Engineered with angstrom-level precision across more than **ten trillion transistors** at a time

17 | Applied Materials External

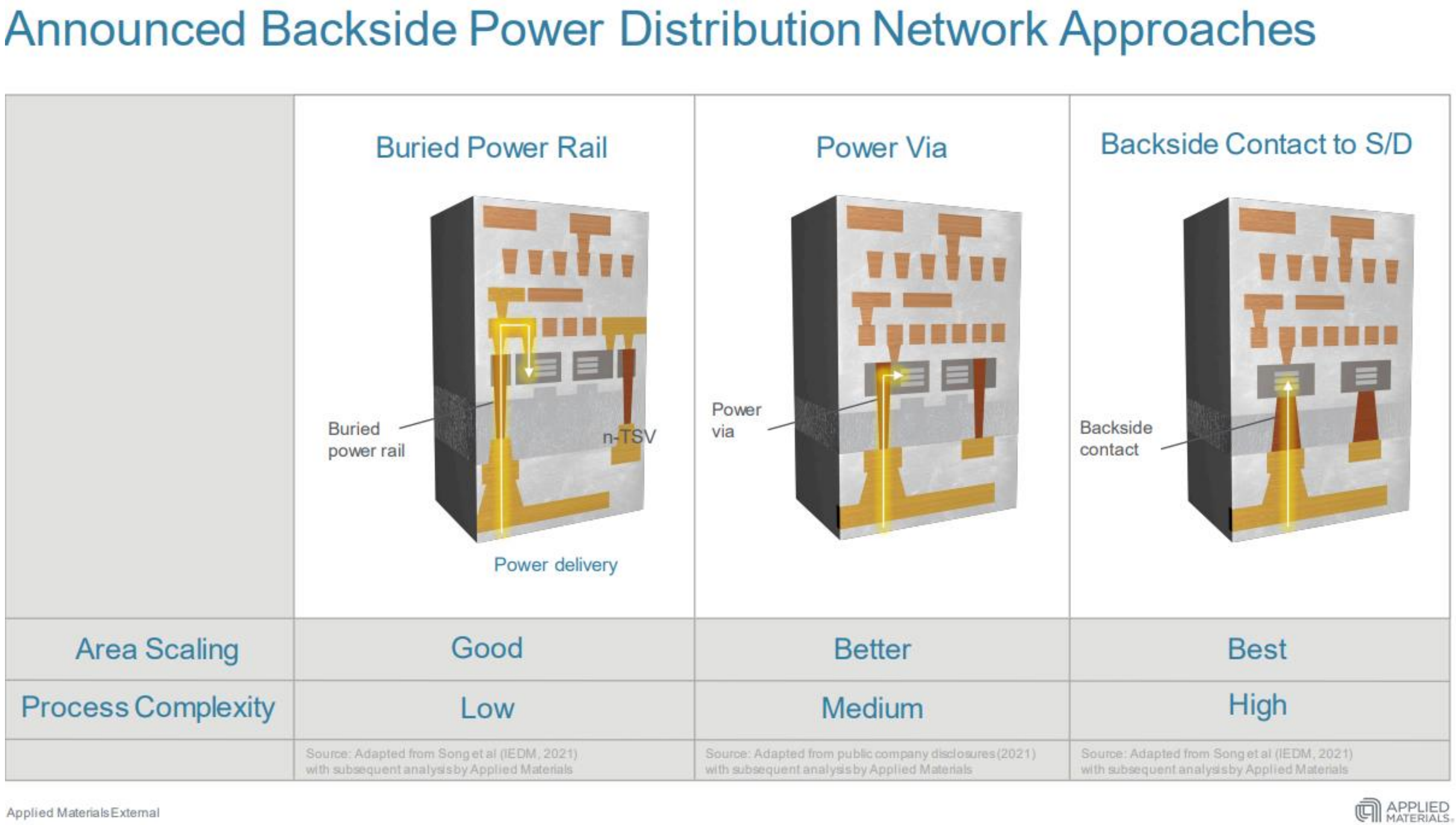
반도체 I Logic





Key changes
- Separation of power and signal lines
- Power delivery from backside of the wafer

Source: Adapted from multiple IMEC and ARM publications

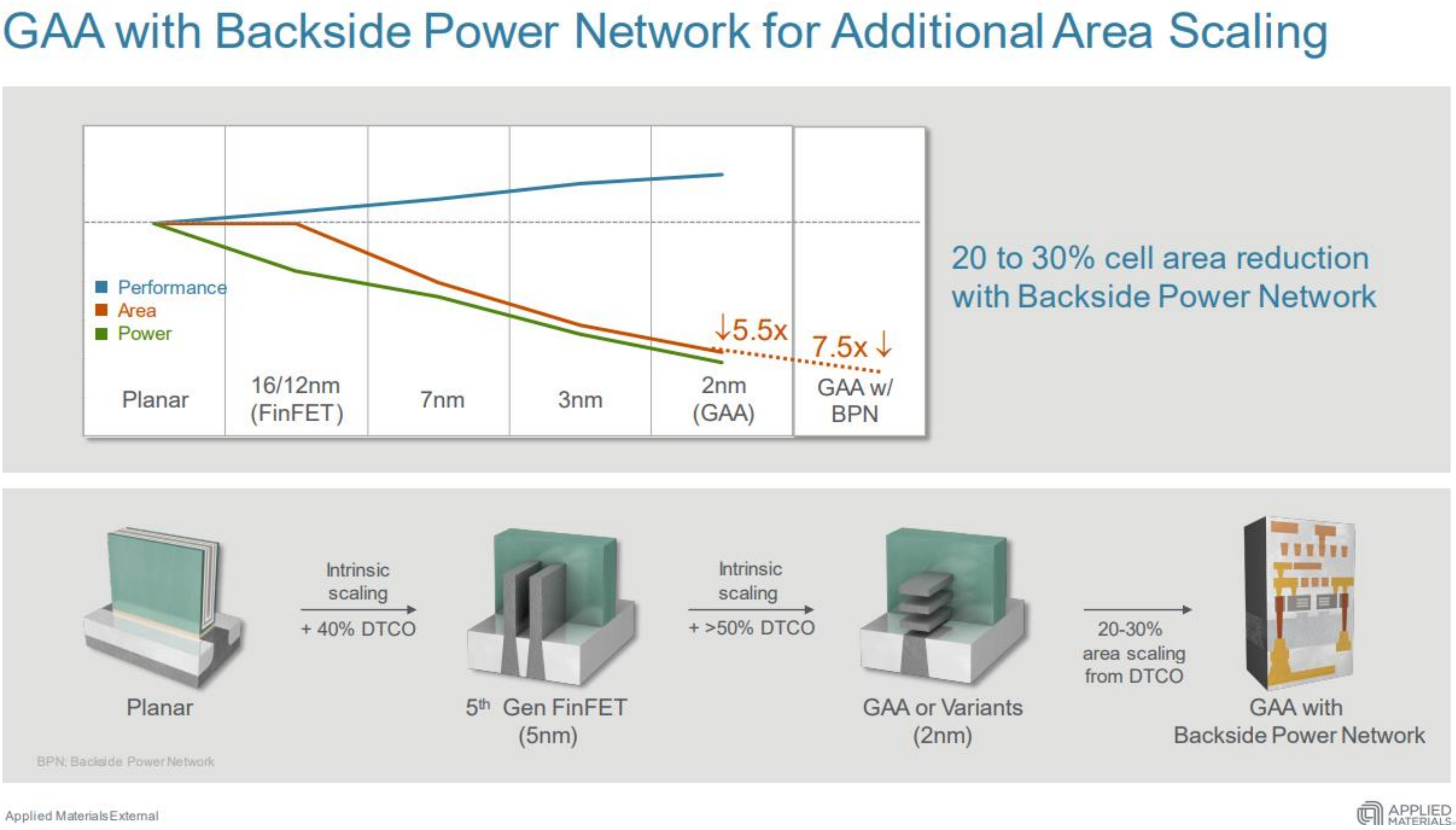


Announced Backside Power Distribution Network Approaches

	Buried Power Rail	Power Via	Backside Contact to S/D
Area Scaling	Good	Better	Best
Process Complexity	Low	Medium	High
	Source: Adapted from Song et al (IEDM, 2021) with subsequent analysis by Applied Materials	Source: Adapted from public company disclosures (2021) with subsequent analysis by Applied Materials	Source: Adapted from Song et al (IEDM, 2021) with subsequent analysis by Applied Materials

Applied Materials External

반도체 | Logic



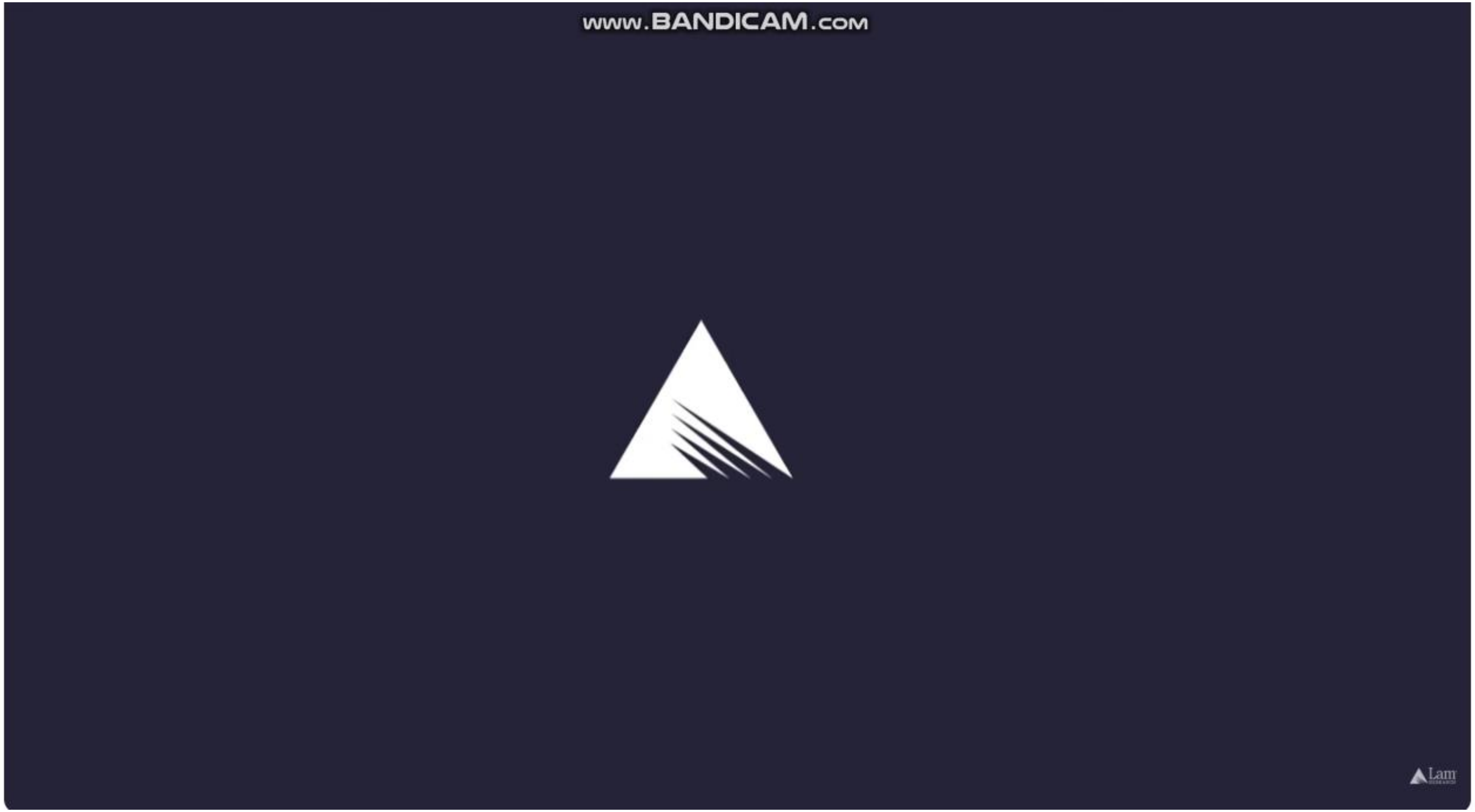
GAA with Backside Power Network for Additional Area Scaling

20 to 30% cell area reduction with Backside Power Network

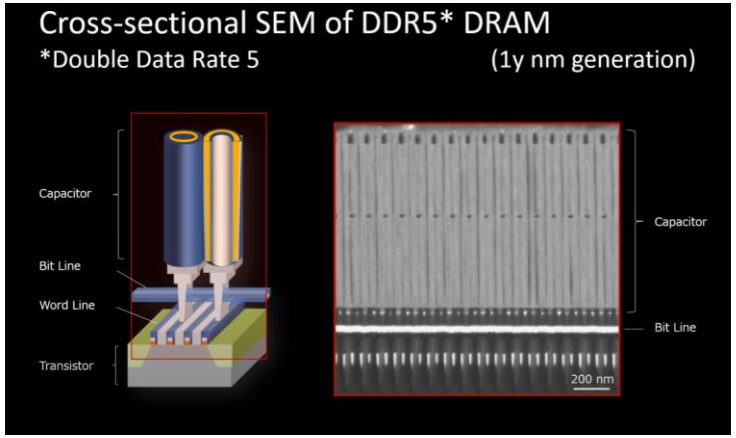
BPN: Backside Power Network

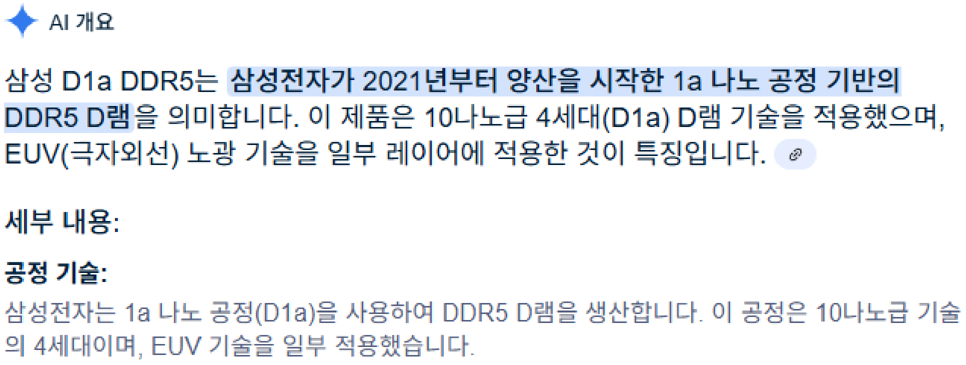
Applied Materials External

반도체 | Logic



반도체 | DRAM



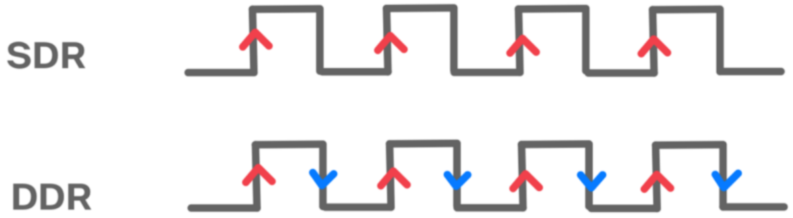


삼성 D1a DDR5는 삼성전자가 2021년부터 양산을 시작한 1a 나노 공정 기반의 DDR5 D램을 의미합니다. 이 제품은 10나노급 4세대(D1a) D램 기술을 적용했으며, EUV(극자외선) 노광 기술을 일부 레이어에 적용한 것이 특징입니다.

세부 내용:

공정 기술:

삼성전자는 1a 나노 공정(D1a)을 사용하여 DDR5 D램을 생산합니다. 이 공정은 10나노급 기술의 4세대이며, EUV 기술을 일부 적용했습니다.

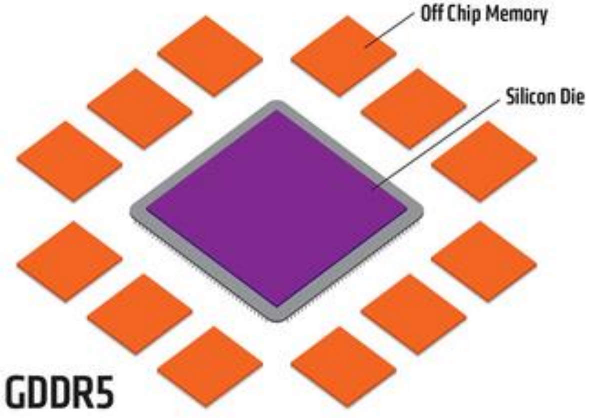


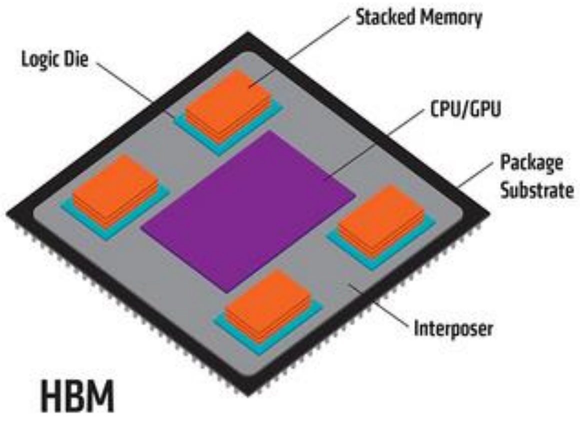
구분	작동전압	단일최대용량	출시년도	전송속도
DDR	2.5 v	2GB	2000	200 ~ 533 MT/s
DDR2	1.8 v	4GB	2003	400 ~ 1066 MT/s
DDR3	1.5 v	8GB	2007	800 ~ 1600 MT/s
DDR4	1.2 v	32GB	2013	1600 ~ 3200 MT/s
DDR5	1.1 v	128GB	2021	3200 ~ 6400 MT/s

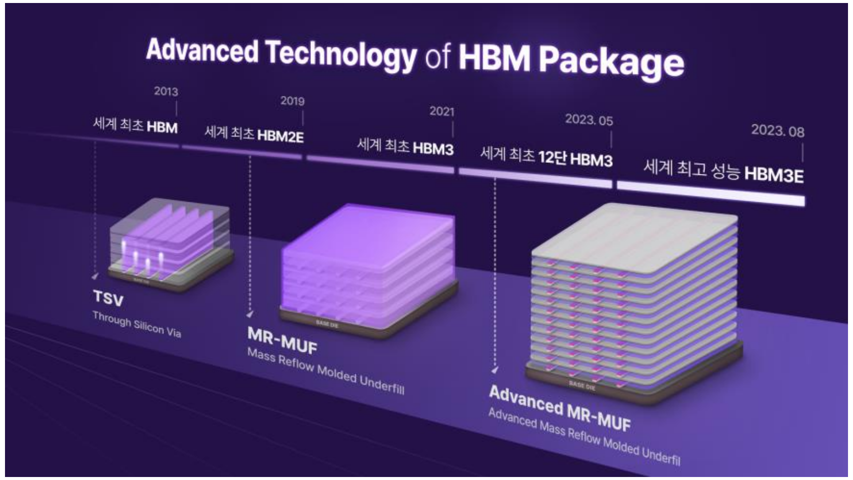
반도체 I DRAM

Original Roadmap

New Technical Roadmap

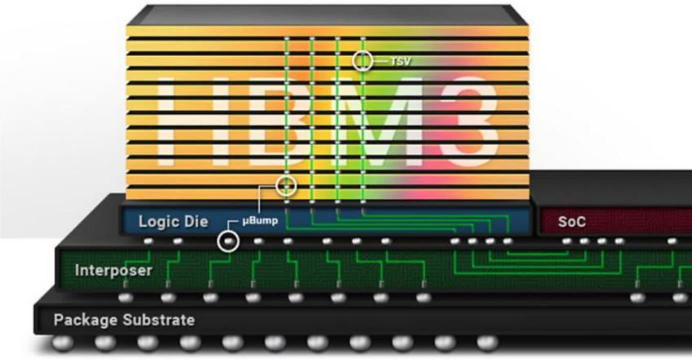


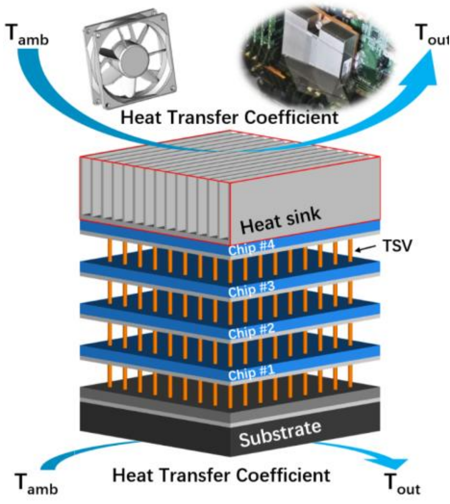




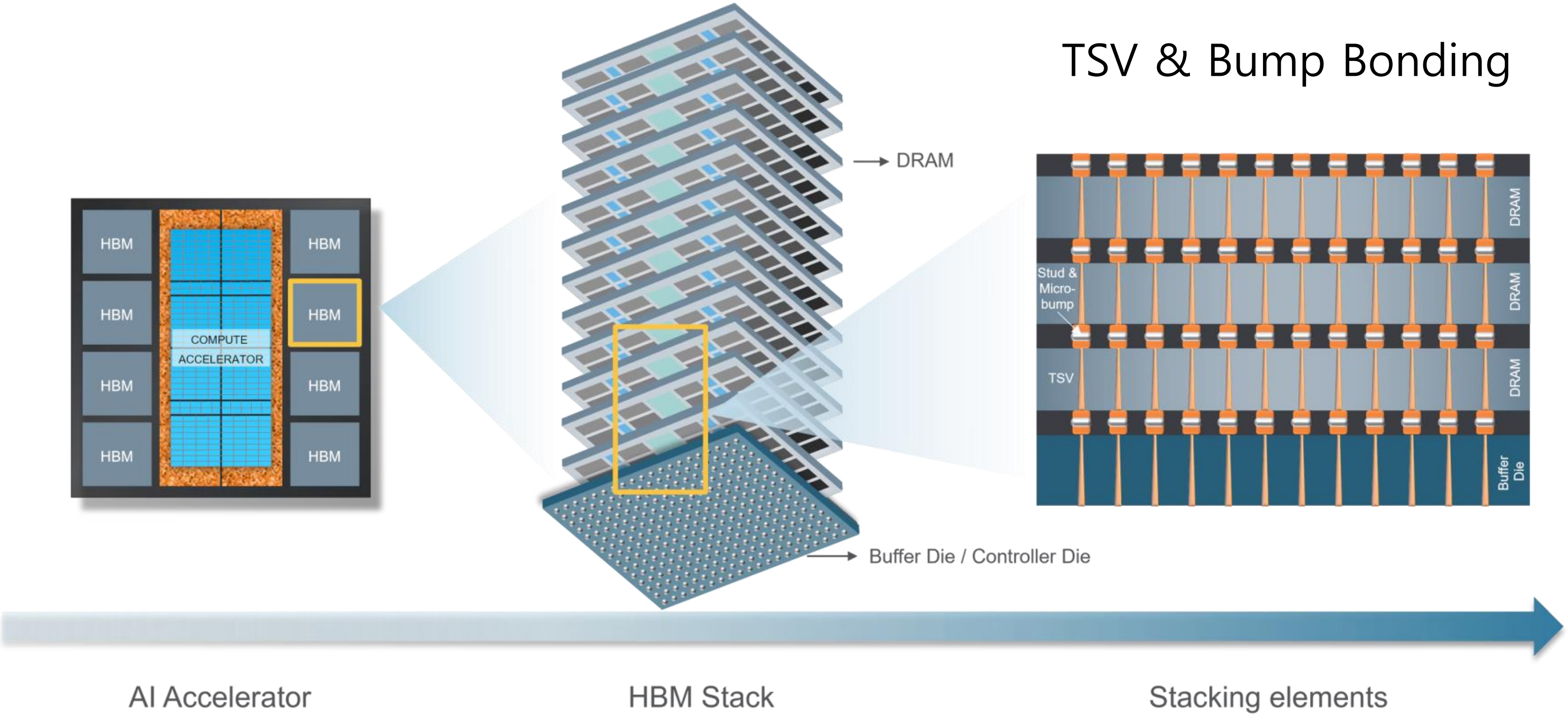
반도체 I DRAM

HBM

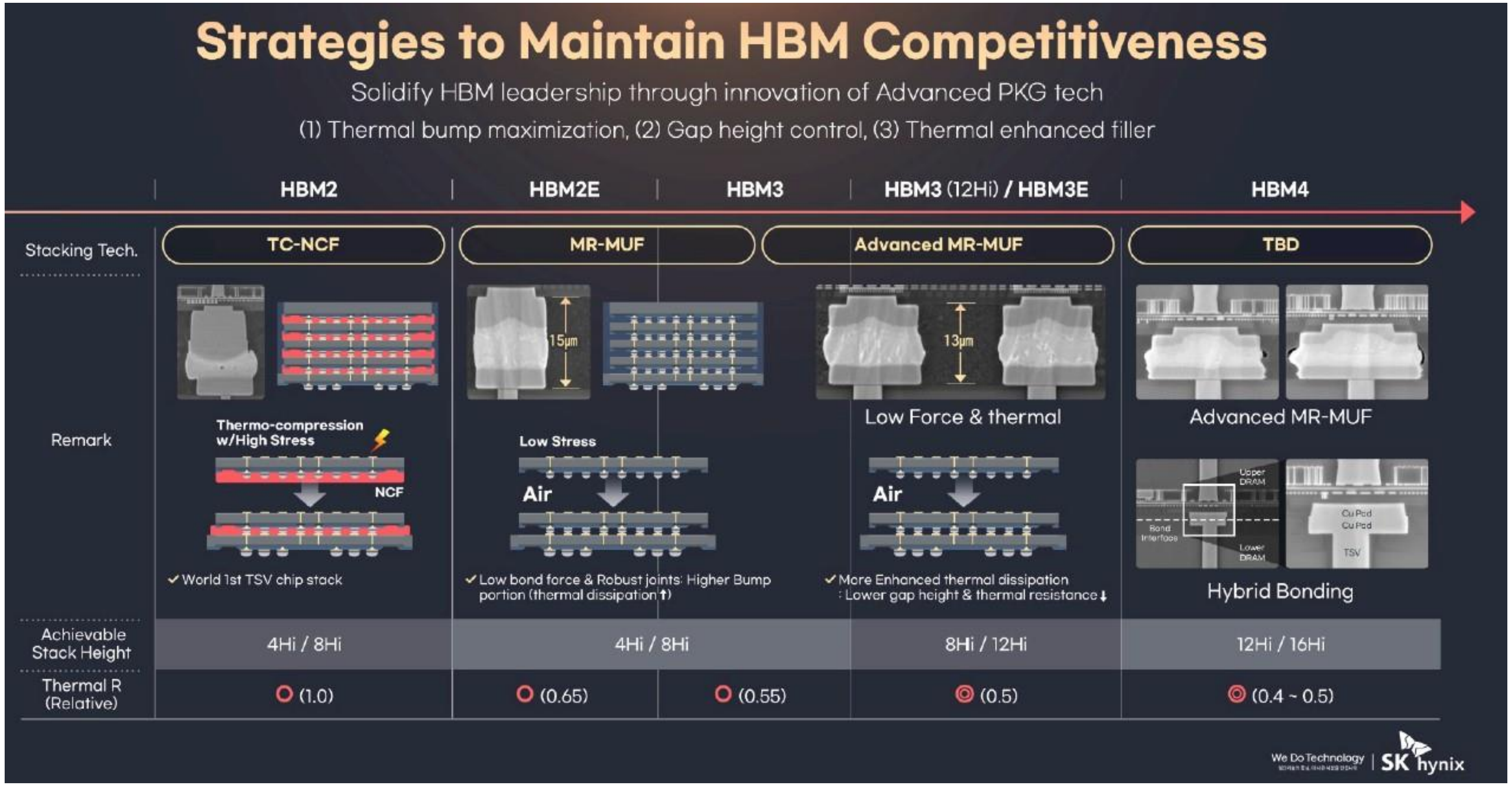




TSV & Bump Bonding



반도체 | DRAM



Strategies to Maintain HBM Competitiveness

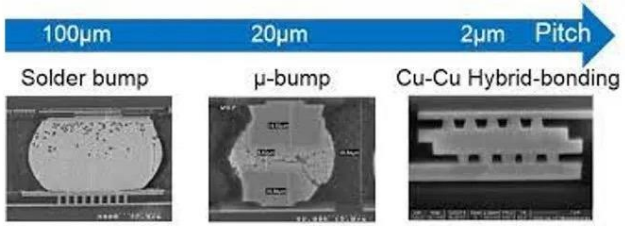
Solidify HBM leadership through innovation of Advanced PKG tech

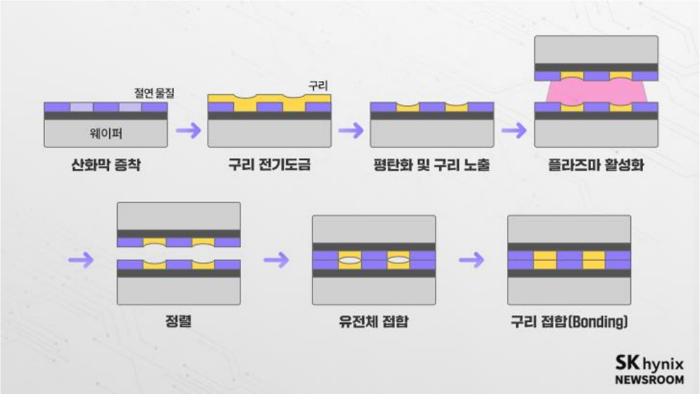
(1) Thermal bump maximization, (2) Gap height control, (3) Thermal enhanced filler

	HBM2	HBM2E	HBM3	HBM3 (12Hi) / HBM3E	HBM4
Stacking Tech.	TC-NCF	MR-MUF		Advanced MR-MUF	TBD
Remark	Thermo-compression w/High Stress NCF ✓ World 1st TSV chip stack	15µm Low Stress Air ✓ Low bond force & Robust joints: Higher Bump portion (thermal dissipation ↑)		13µm Low Force & thermal Air ✓ More Enhanced thermal dissipation : Lower gap height & thermal resistance ↓	Advanced MR-MUF Hybrid Bonding
Achievable Stack Height	4Hi / 8Hi	4Hi / 8Hi		8Hi / 12Hi	12Hi / 16Hi
Thermal R (Relative)	○ (1.0)	○ (0.65)	○ (0.55)	◎ (0.5)	◎ (0.4 ~ 0.5)

We Do Technology | SK hynix

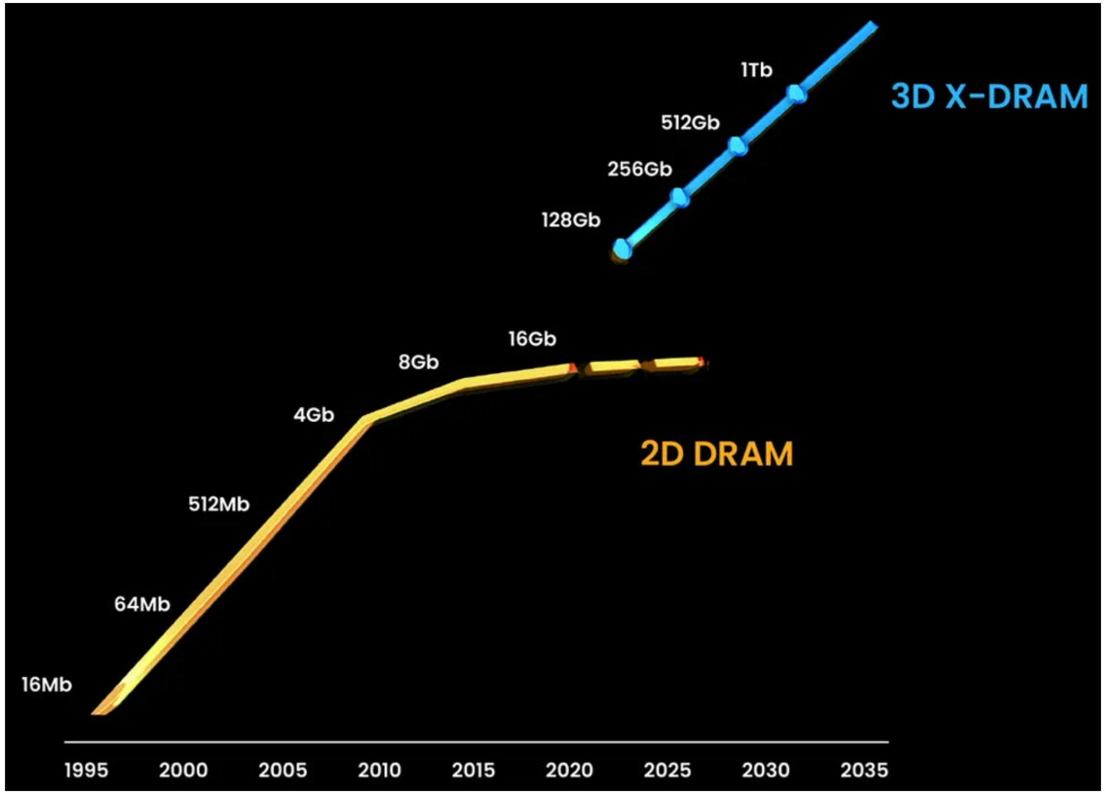
Hybrid Cu Bonding

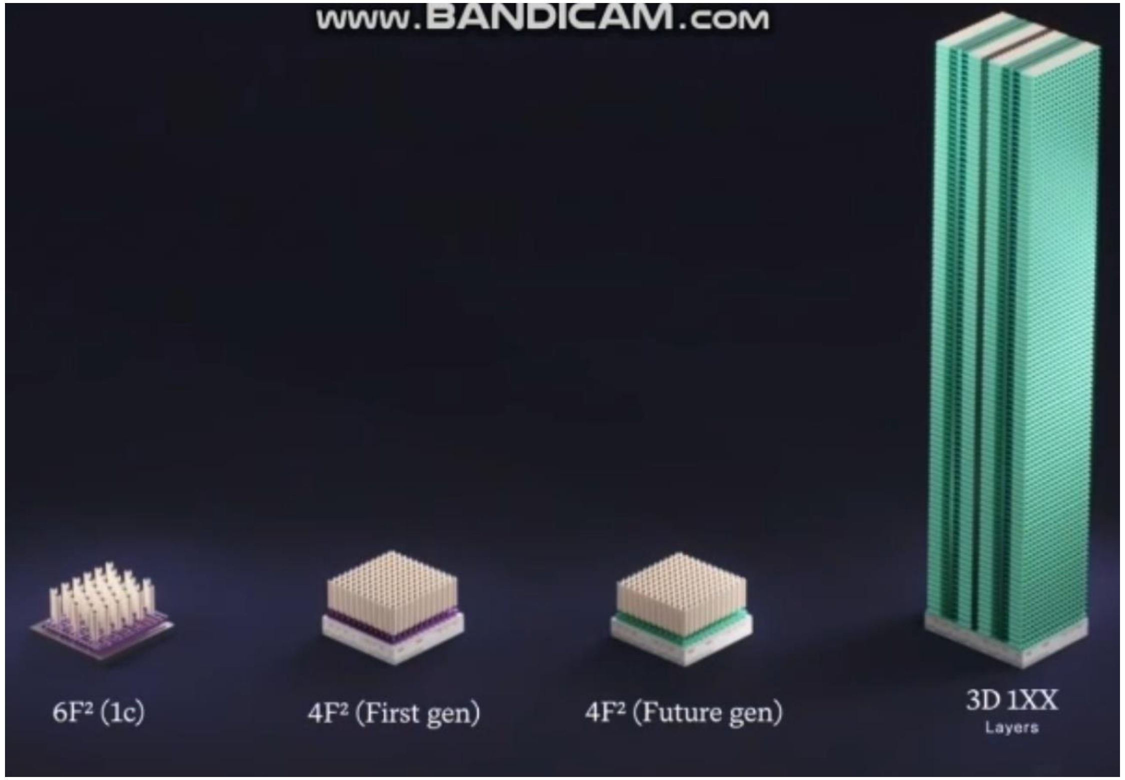




반도체 I DRAM

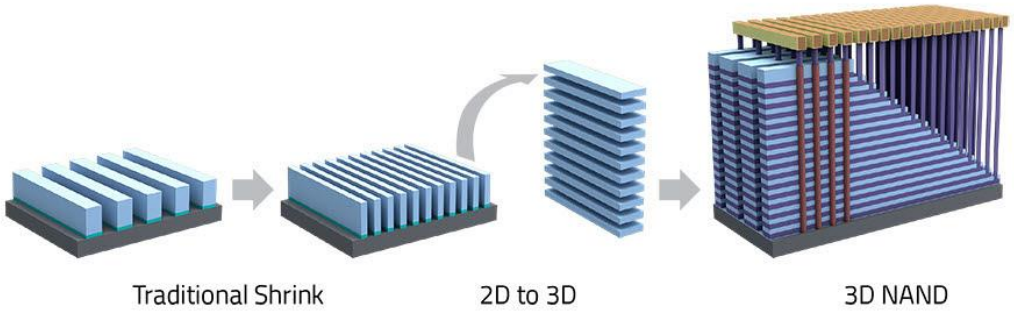
반도체 I DRAM

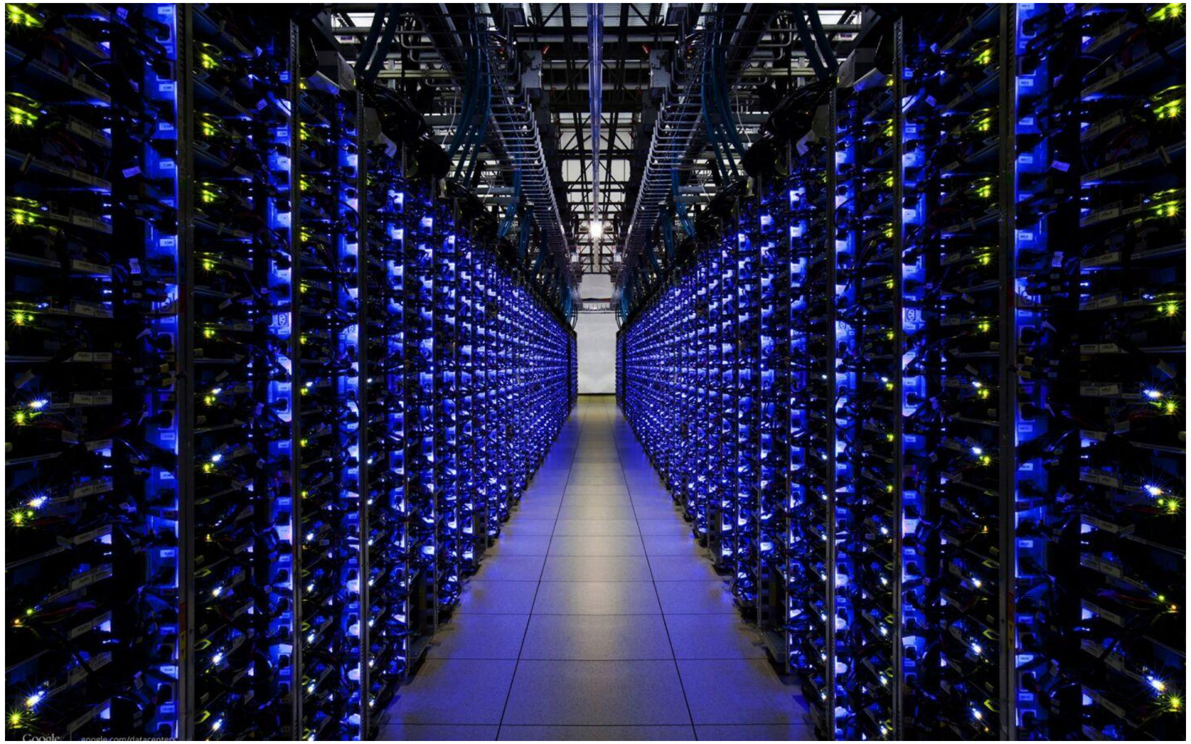




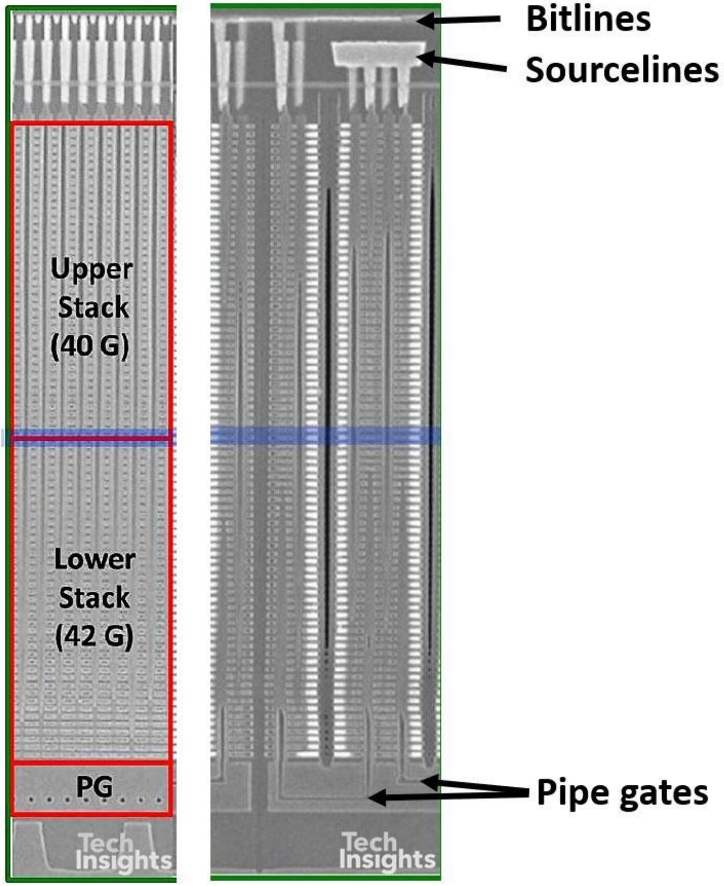
https://www.tomshardware.com/news/3d-x-dram-roadmap-1tb-die-density-by-2030

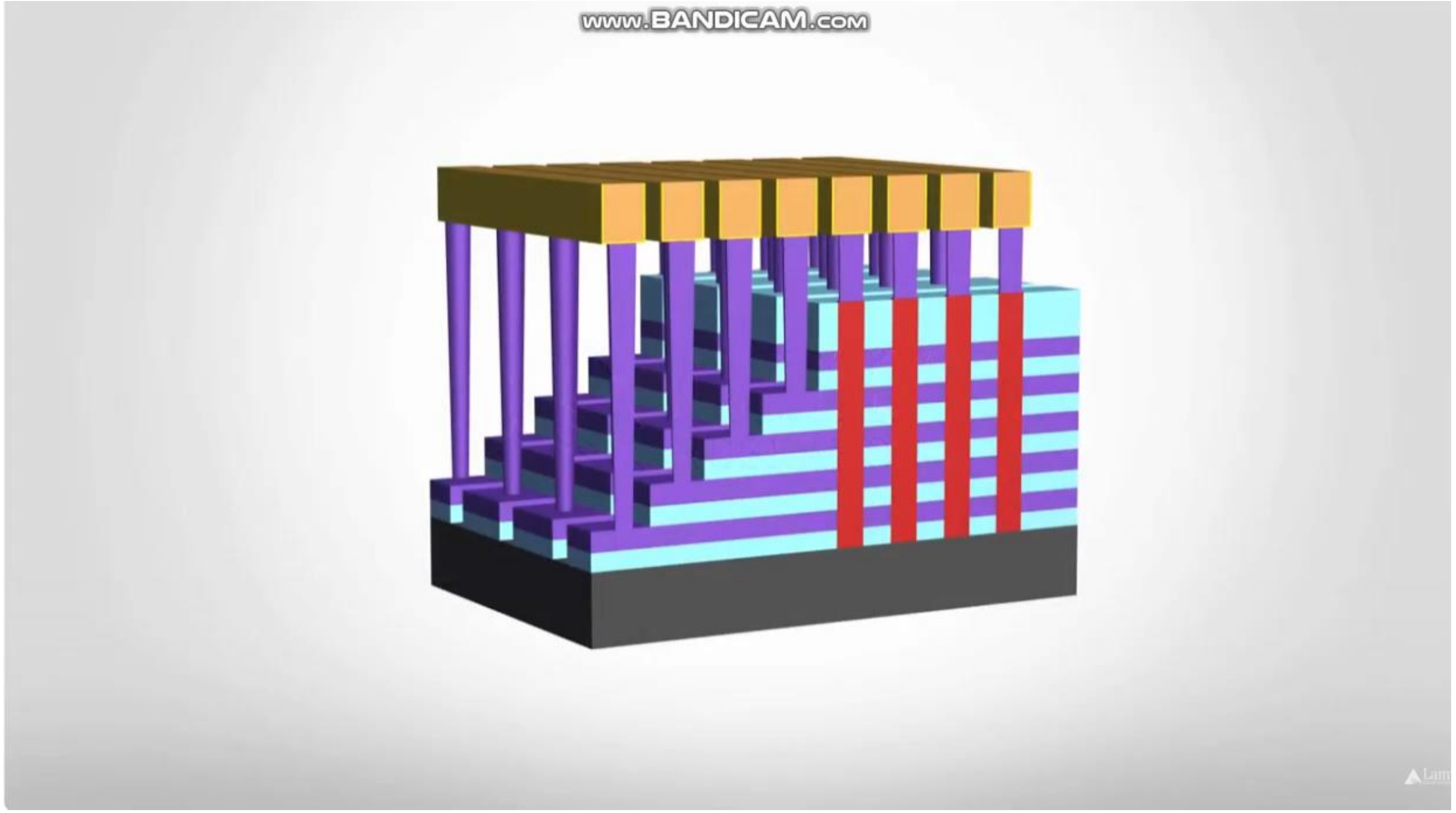
반도체 I NAND





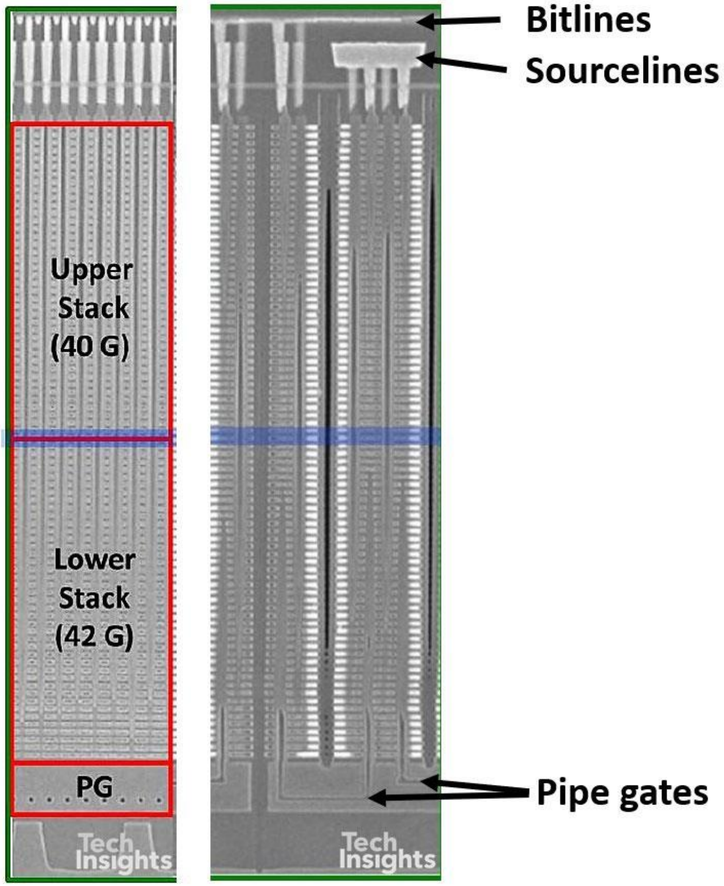
반도체 I NAND

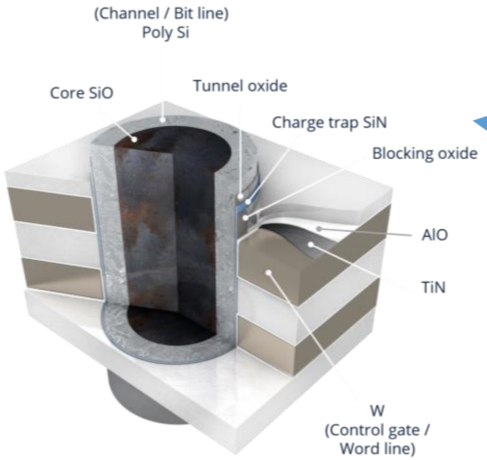




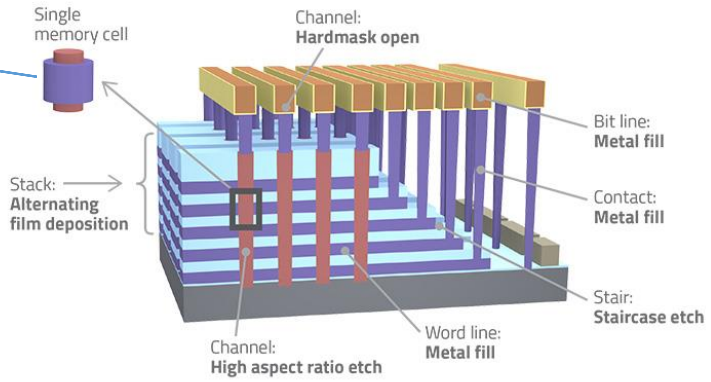
https://www.techinsights.com/blog/techinsights-memory-technology-update-iedm18?utm_source=direct&utm_medium=website
https://newsroom.lamresearch.com/Tech-Brief-Memory-Grows-Up-with-3D-NANDt
https://www.appliedmaterials.com/us/en/semiconductor/markets-and-inflections/memory/3d-nand.html

반도체 | NAND

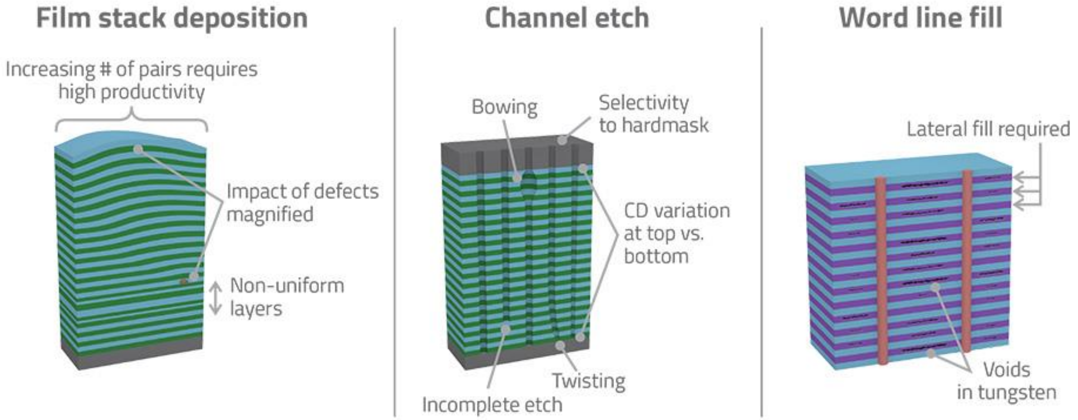




Key Process Steps in 3D NAND Memory Cell Formation

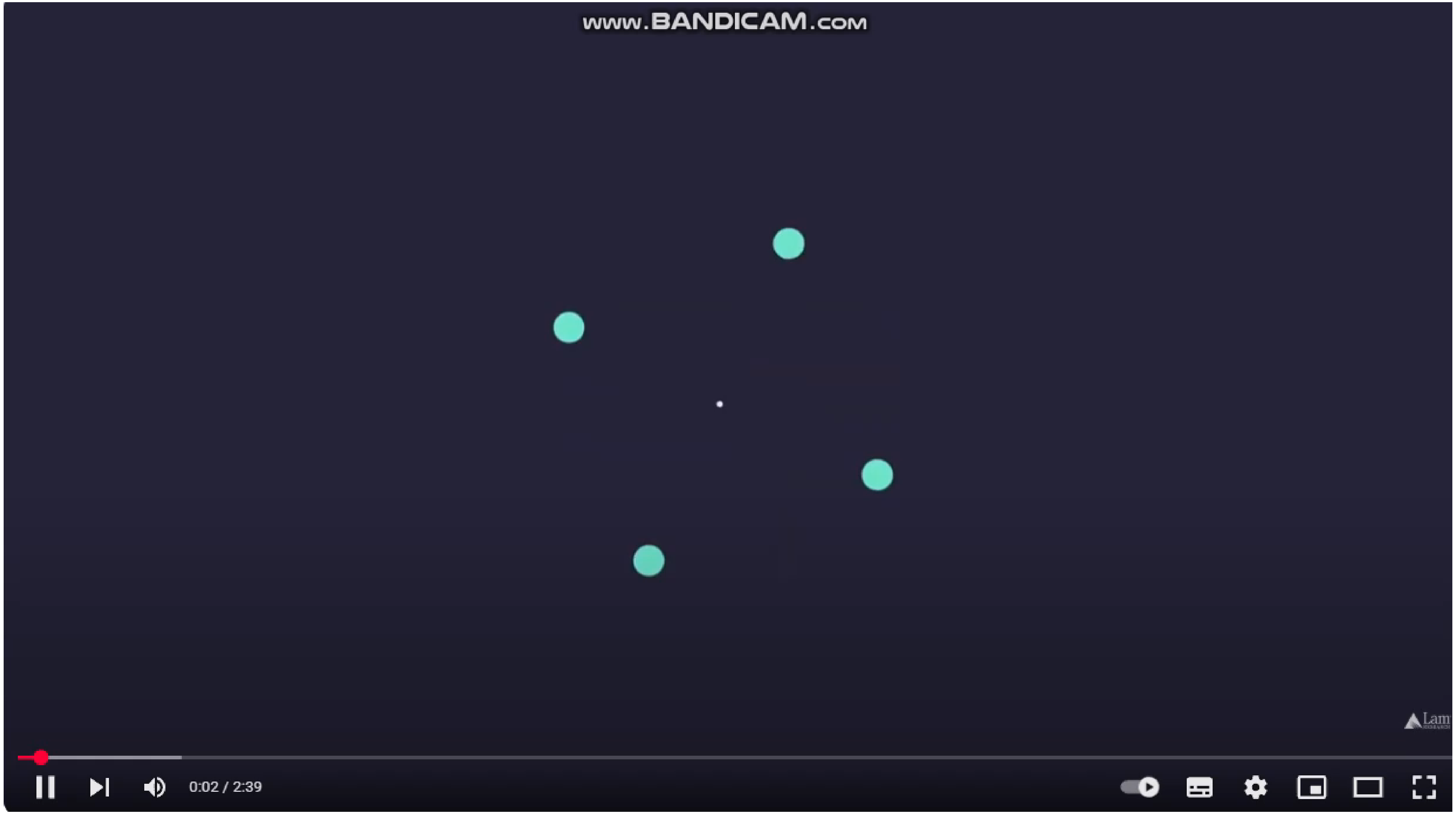


3D NAND Manufacturing Challenges

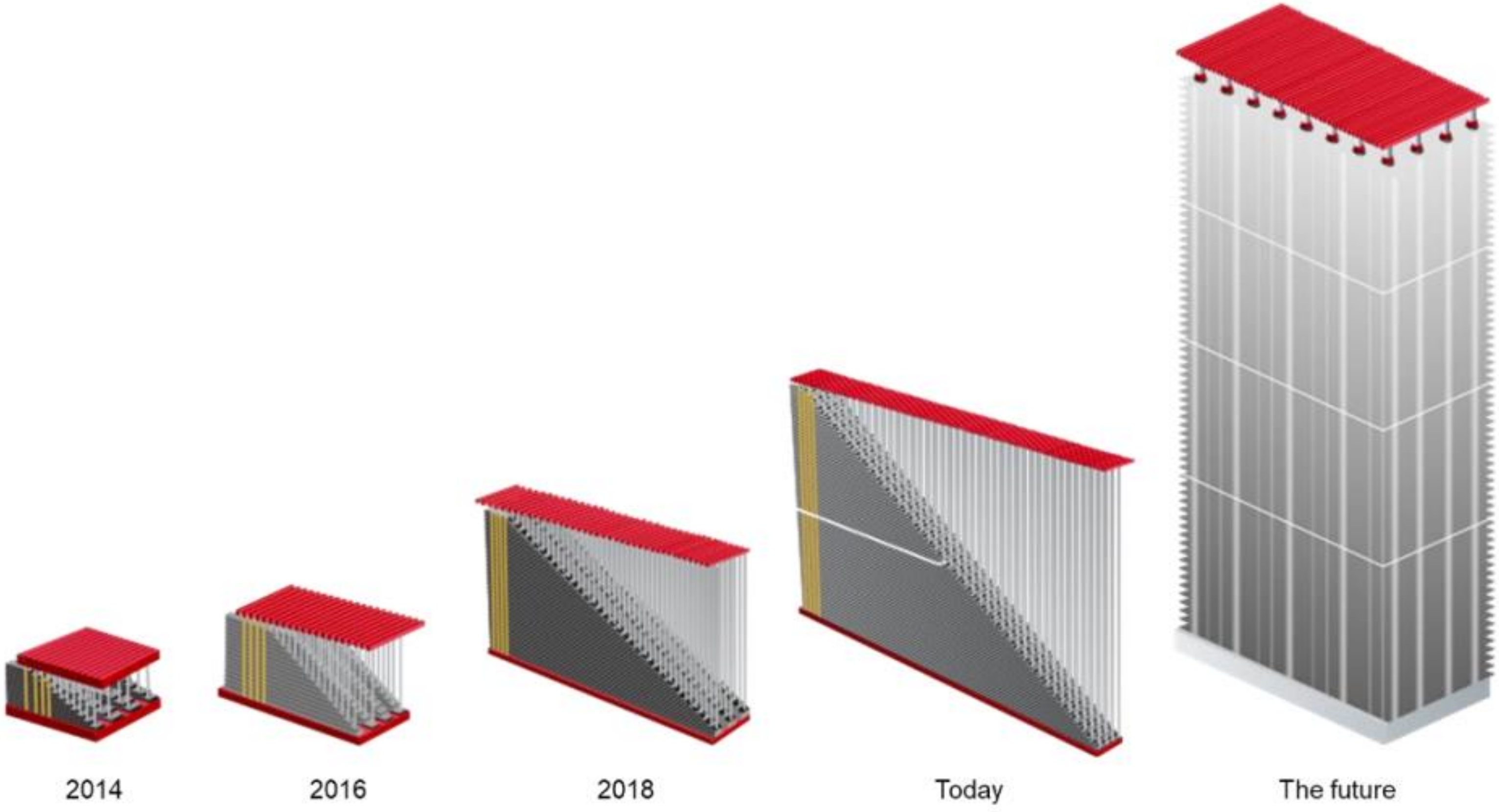


https://www.techinsights.com/blog/techinsights-memory-technology-update-iedm18?utm_source=direct&utm_medium=website
https://newsroom.lamresearch.com/Tech-Brief-Memory-Grows-Up-with-3D-NANDt
https://www.appliedmaterials.com/us/en/semiconductor/markets-and-inflections/memory/3d-nand.html

반도체 I NAND

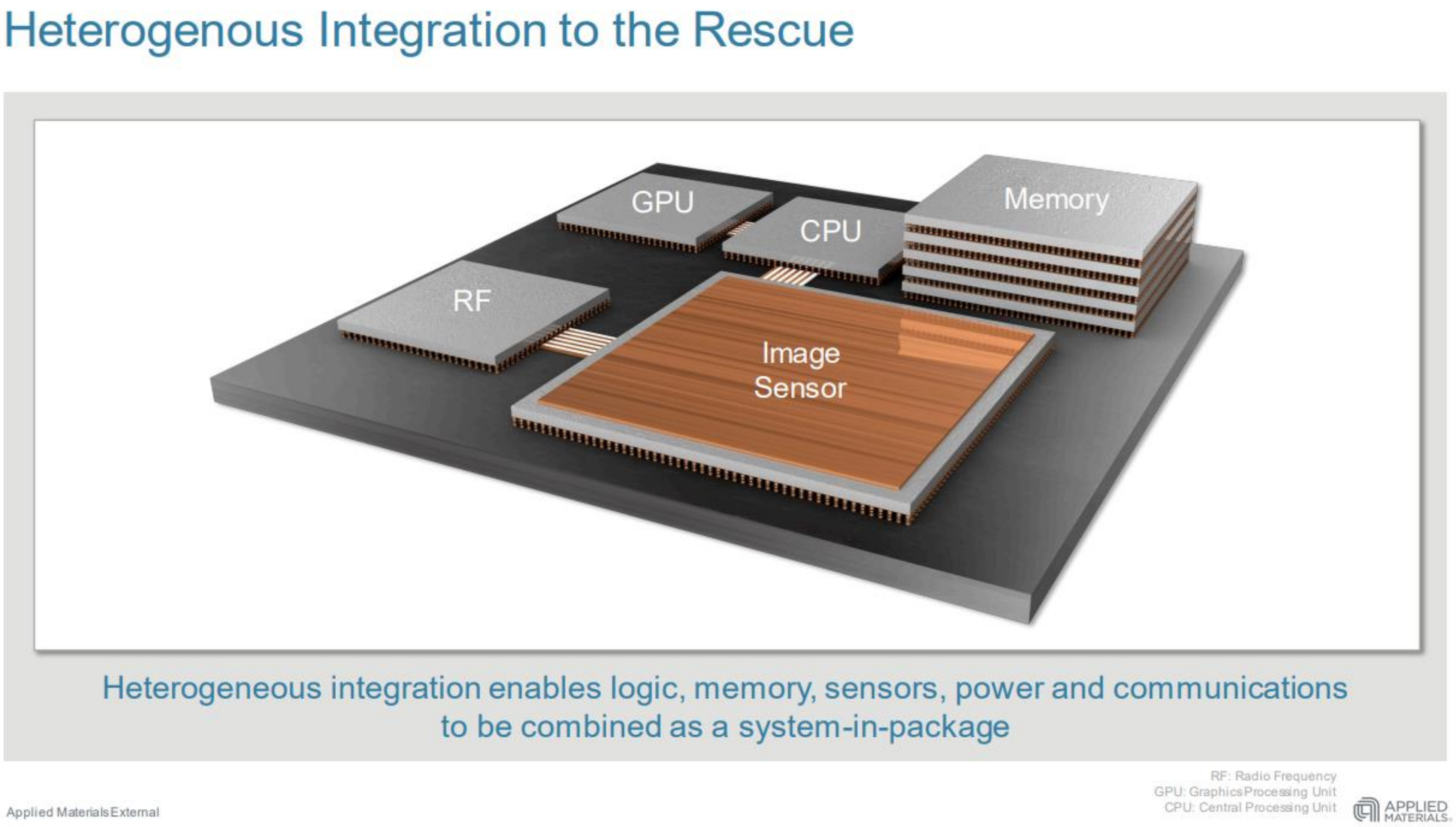


반도체 I NAND



Sources: Lam Research, Counterpoint Research

반도체 I Advanced Packaging

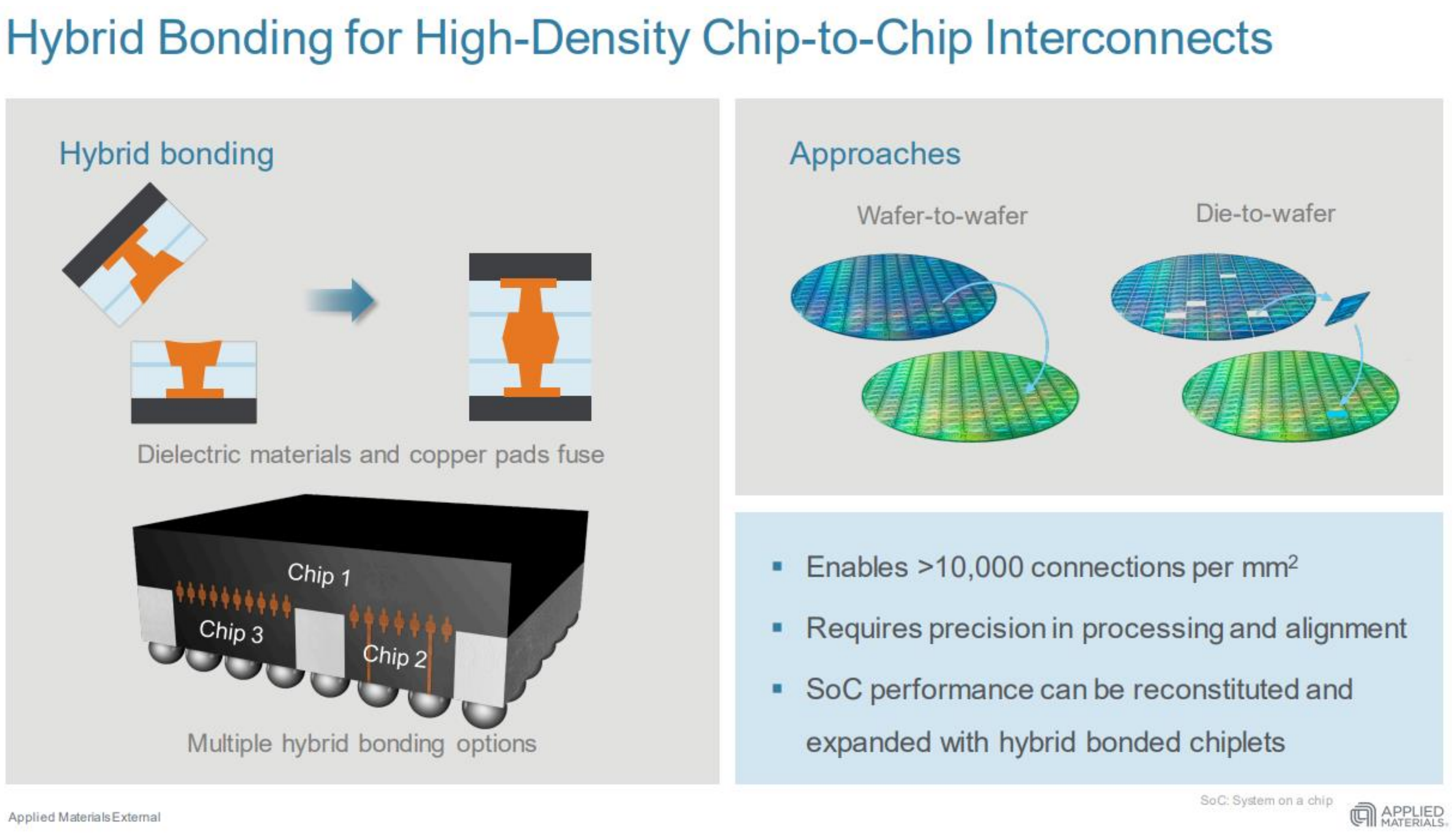


Heterogenous Integration to the Rescue

Heterogeneous integration enables logic, memory, sensors, power and communications to be combined as a system-in-package

RF: Radio Frequency
GPU: Graphics Processing Unit
CPU: Central Processing Unit

반도체 I Advanced Packaging



Hybrid Bonding for High-Density Chip-to-Chip Interconnects

Hybrid bonding

Dielectric materials and copper pads fuse

Multiple hybrid bonding options

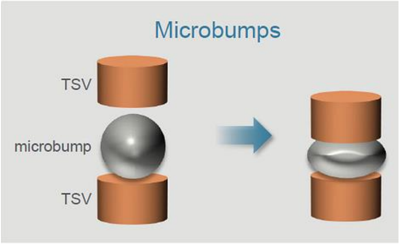
Approaches

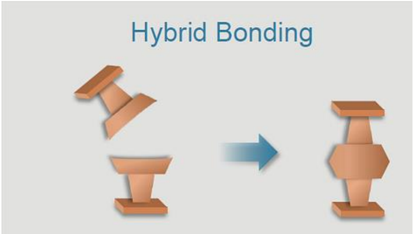
- Enables >10,000 connections per mm^2
- Requires precision in processing and alignment
- SoC performance can be reconstituted and expanded with hybrid bonded chiplets

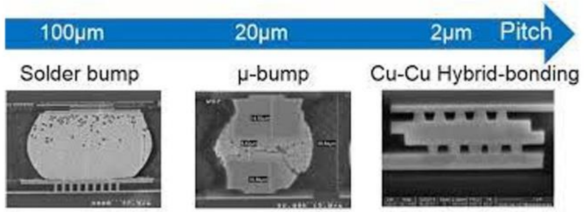
Applied Materials External

SoC: System on a chip

APPLIED MATERIALS







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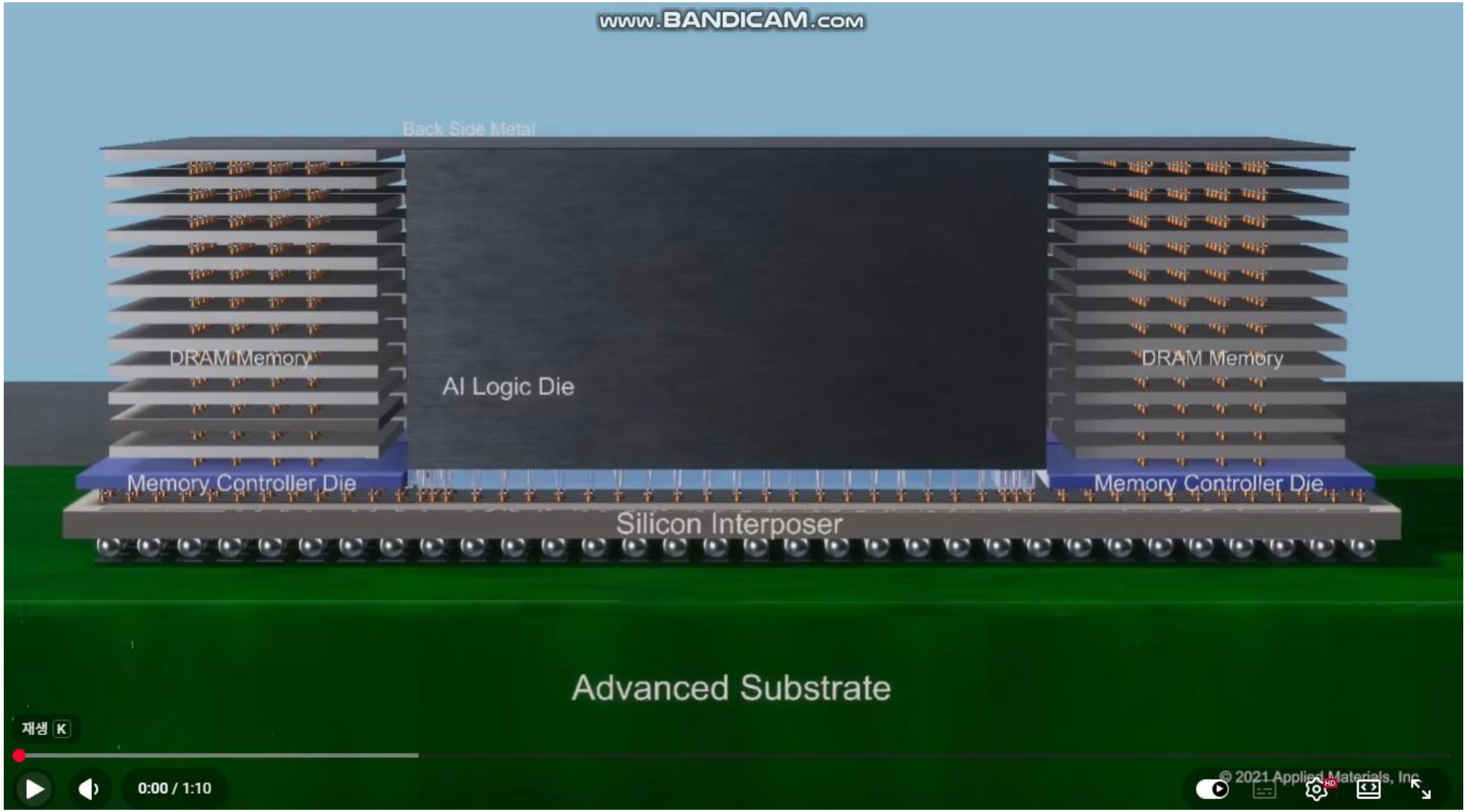
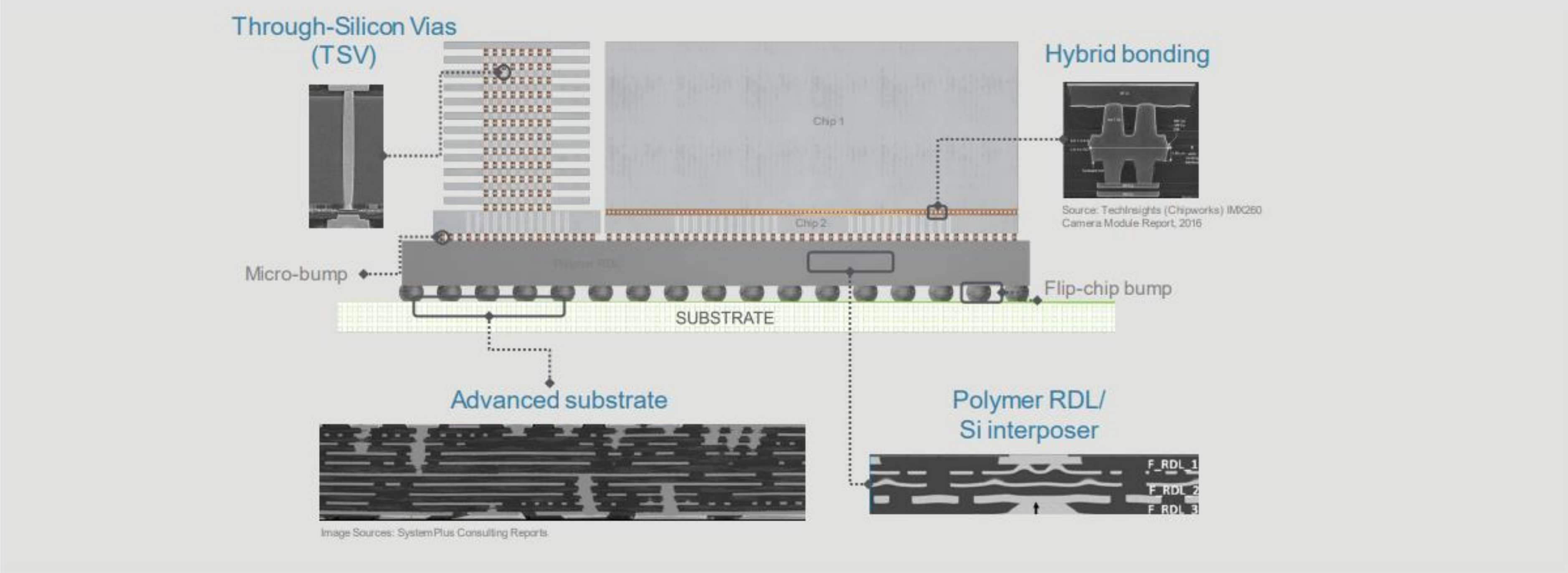


반도체 I Advanced Packaging

System Integration with Emerging 2D and 3D Interconnects



Source: TechInsights (Chipworks) IMX260 Camera Module Report, 2016

Image Sources: System Plus Consulting Reports

- Advanced substrates package chips side-by-side with higher bandwidth (more I/Os) and lower power
- TSVs with micro-bumps or hybrid bonding create vertical interconnects allowing chip-on-chip stacking

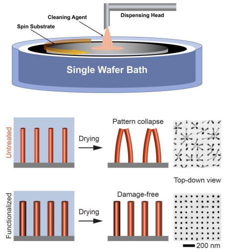
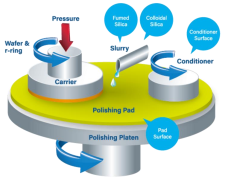
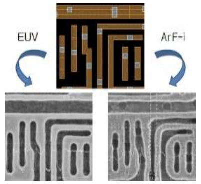
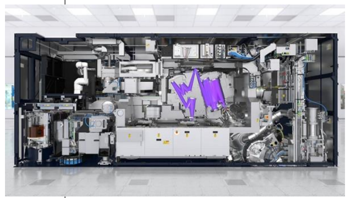
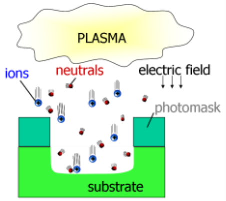
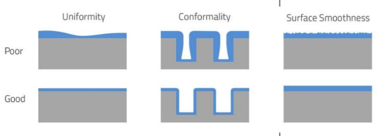
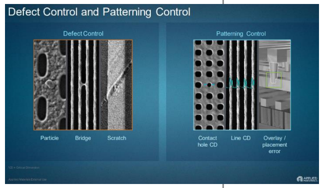
반도체
Unit Process

Intro | 반도체 Workflow

Device & Process Design → Unit Process → 수율 및 불량 분석 → Packaging

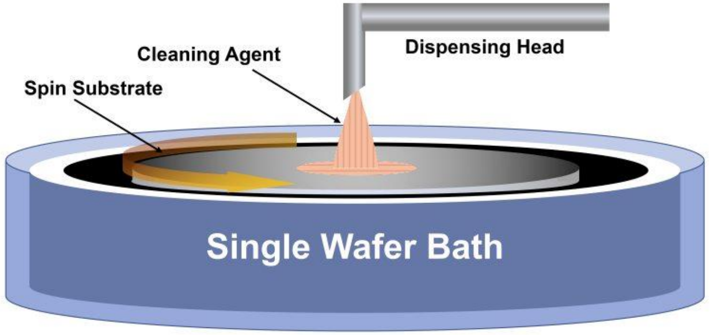
8대 공정 : Clean, CMP, Photo (Litho), Etch, Depo, Inspection & Metrology

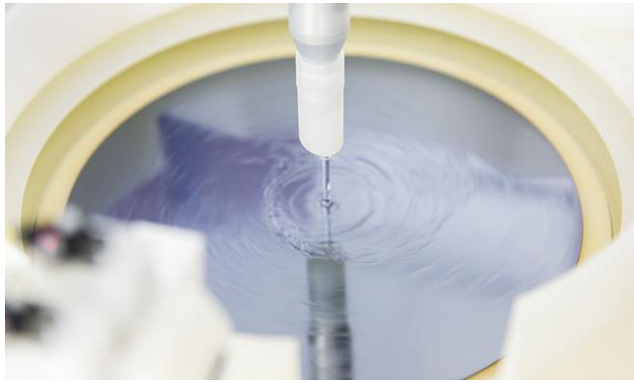
준비 → 패턴 → 증착 → 검사

공정	세정 (Wet Clean)	평탄화 (CMP)	PR 도포/현상 (Spinner)	노광 (Photo-Litho)	식각 (Etch)	증착 (Depo)	검사
회사	SCREEN TEL	APPLIED MATERIALS	TEL	ASML	Lam RESEARCH APPLIED MATERIALS TEL	APPLIED MATERIALS	APPLIED MATERIALS KLA HITACHI Inspire the Next
기술	나노 파티클 제거, 초임계, 공학 (로봇 등)	Slurry, Warpage	Spin 코팅, 현상, 공학 (로봇 등)	KrF, ArF, EUV (파장), 분해능	Plasma Etch, ALE, Selective Etch	CVD, PECVD, ALD	광학, E-beam
							

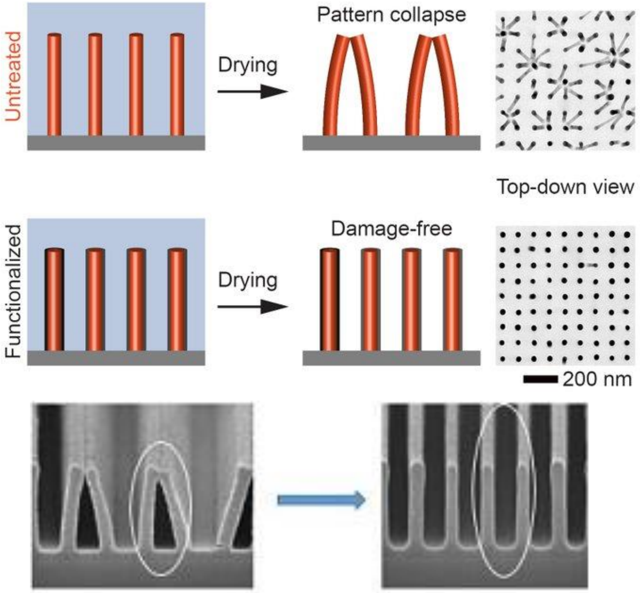
반도체 | Unit Process - Clean

공정	세정 (Wet Clean)
회사	SCREEN TEL SEMES
기술	나노 파티클 제거, 초임계, 공학 (로봇 등)



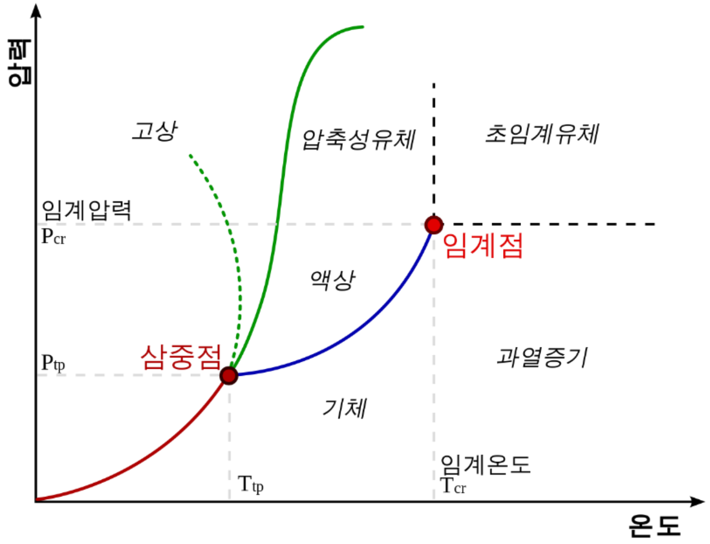


리닝 (Leaning)



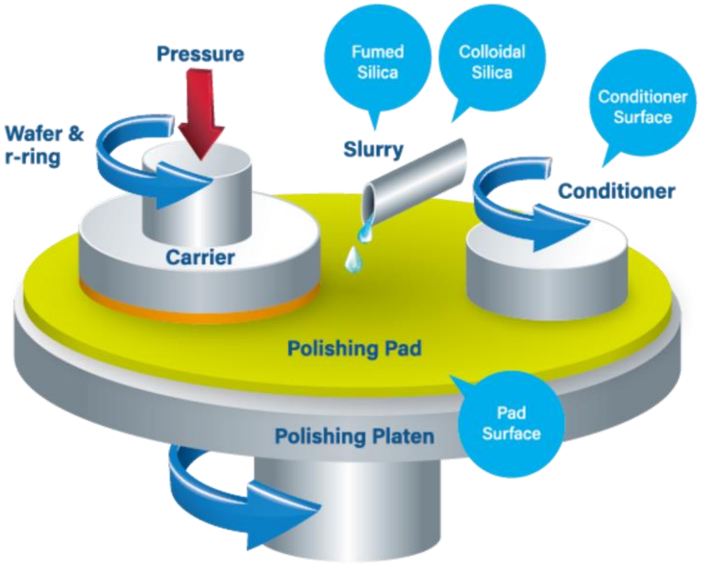
액체 표면에너지

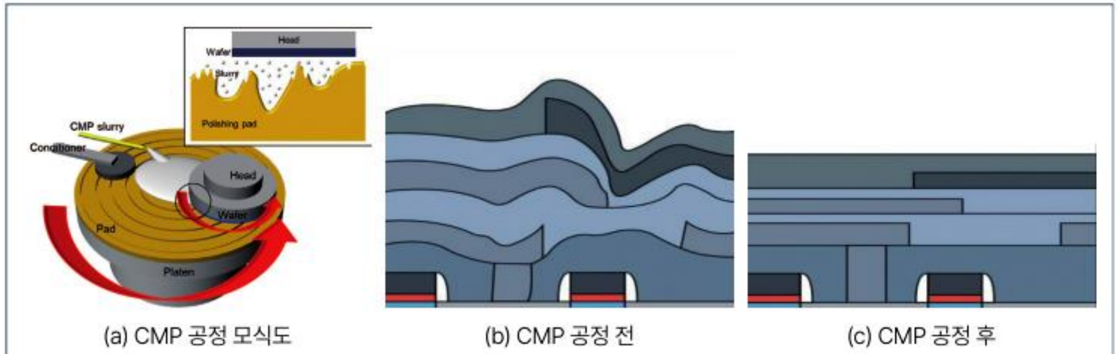
초임계 유체 기술



반도체 I Unit Process - CMP

공정	평탄화 (CMP)
회사	APPLIED MATERIALS
기술	Slurry, Warpage

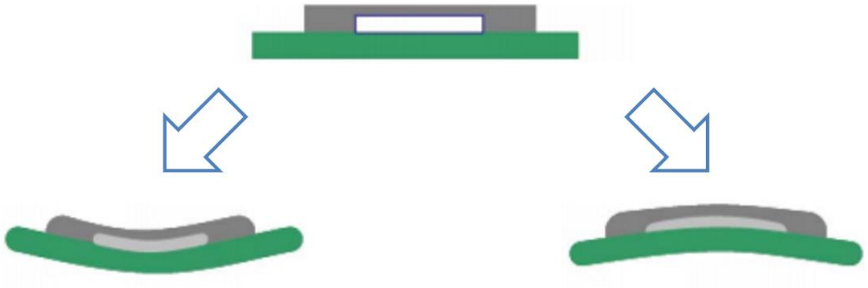




(a) CMP 공정 모식도 (b) CMP 공정 전 (c) CMP 공정 후

<그림 1> CMP 공정 개요 및 CMP 전/후 소자 구자 구조의 변화

Warpage Wafer

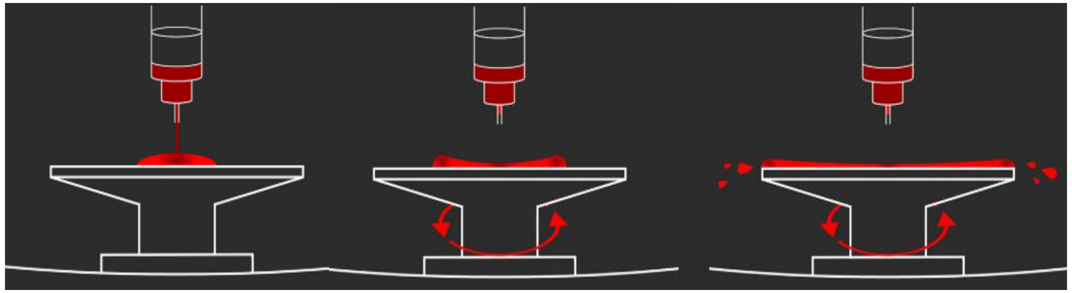


Smiling Warpage

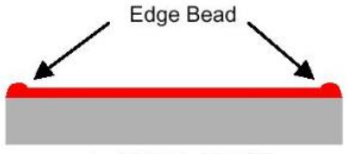
Crying Warpage

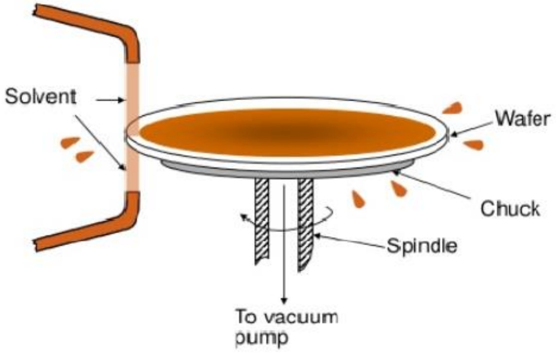
반도체 | Unit Process - Spinner

Conventional
: CAR PR (Chemical Amplification Resist)

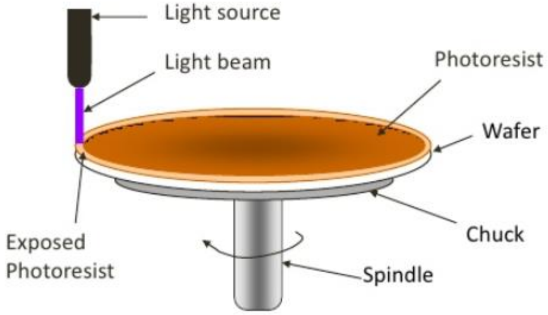


공정	**PR 도포/현상 (Spinner)**
회사	TEL
기술	Spin 코팅, 현상, 공학 (로봇 등)





<Edge Bead removal with solvent>



<Edge Bead removal with optical method>

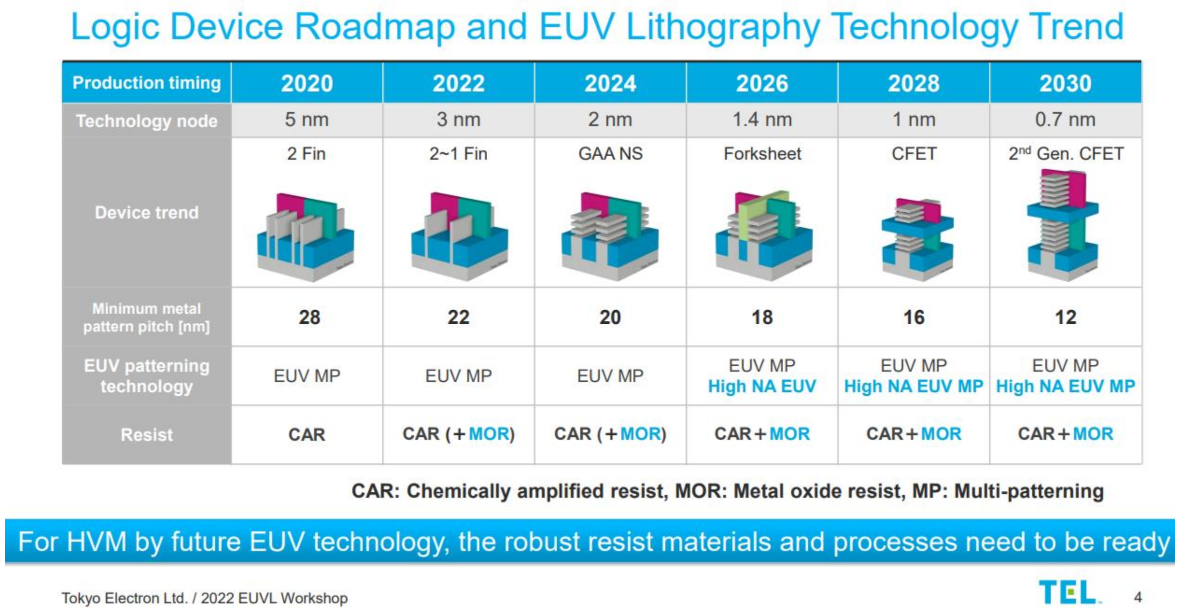
반도체 I Unit Process

EUV
: MOR PR (Metal Oxide Resist)

*금속 원소 (Sn, Zr, Hf 등) 함유

JSR JSR Corporation inpria

공정	PR 도포/현상 (Spinner)
회사	TEL
기술	Spin 코팅, 현상, 공학 (로봇 등)



Logic Device Roadmap and EUV Lithography Technology Trend

Production timing	2020	2022	2024	2026	2028	2030
Technology node	5 nm	3 nm	2 nm	1.4 nm	1 nm	0.7 nm
Device trend	2 Fin	2~1 Fin	GAA NS	Forksheet	CFET	2nd Gen. CFET
Minimum metal pattern pitch [nm]	28	22	20	18	16	12
EUV patterning technology	EUV MP	EUV MP	EUV MP	EUV MP High NA EUV	EUV MP High NA EUV MP	EUV MP High NA EUV MP
Resist	CAR	CAR (+MOR)	CAR (+MOR)	CAR+MOR	CAR+MOR	CAR+MOR

CAR: Chemically amplified resist, MOR: Metal oxide resist, MP: Multi-patterning

For HVM by future EUV technology, the robust resist materials and processes need to be ready

Tokyo Electron Ltd. / 2022 EUVL Workshop

TEL 4

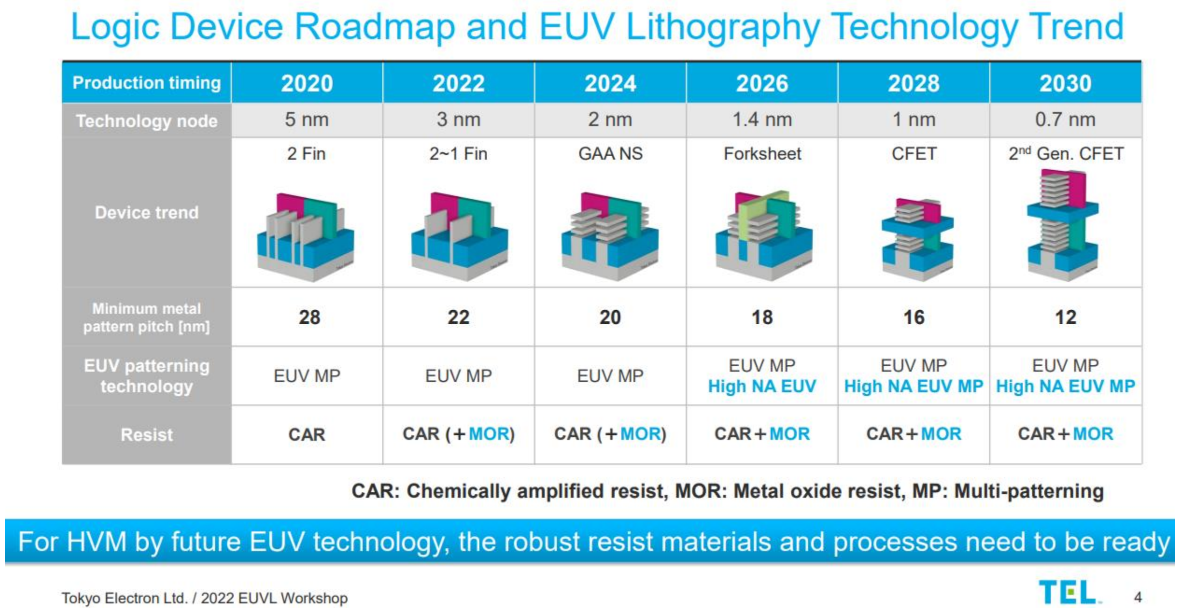
반도체 | Unit Process

EUV
: MOR PR (Metal Oxide Resist)

*금속 원소 (Sn, Zr, Hf 등) 함유

JSR Corporation inpria

공정	PR 도포/현상 (Spinner)
회사	TEL
기술	Spin 코팅, 현상, 공학 (로봇 등)



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EUV patterning technology	EUV MP	EUV MP	EUV MP	EUV MP High NA EUV	EUV MP High NA EUV MP	EUV MP High NA EUV MP
Resist	CAR	CAR (+MOR)	CAR (+MOR)	CAR+MOR	CAR+MOR	CAR+MOR

CAR: Chemically amplified resist, MOR: Metal oxide resist, MP: Multi-patterning

For HVM by future EUV technology, the robust resist materials and processes need to be ready

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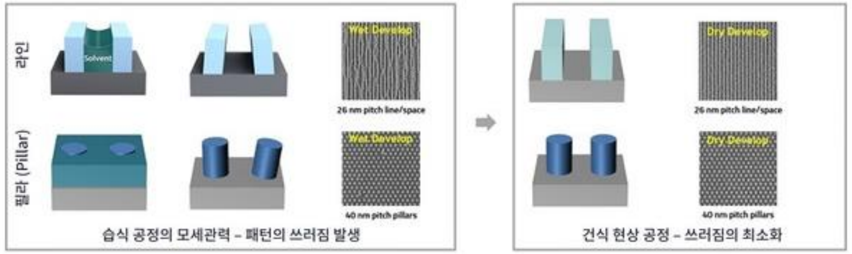
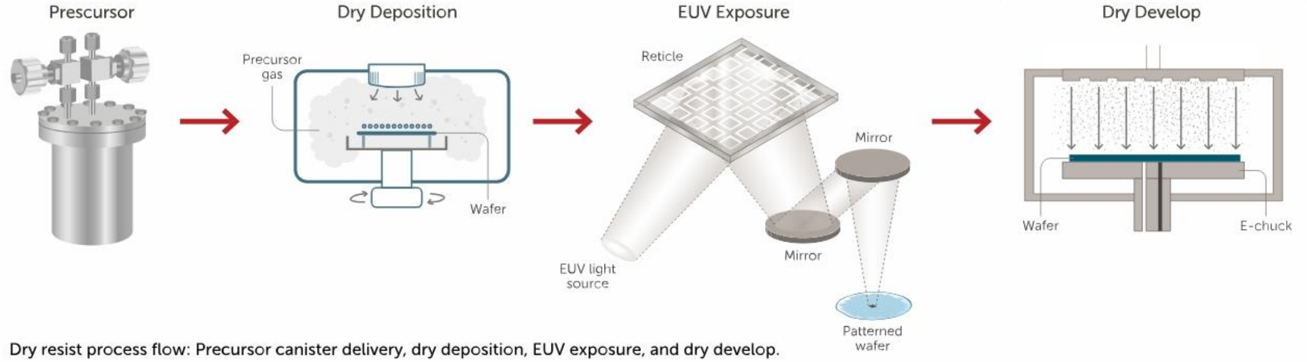
램리서치, 증착으로 EUV PR 만드는 '드라이 레지스트' 개발…日 기술 대체 촉각

발행일 : 2020-02-27 19:07 지면 : 2020-02-28 21면



습식 공정의 모세관력 – 패턴의 쓰러짐 발생

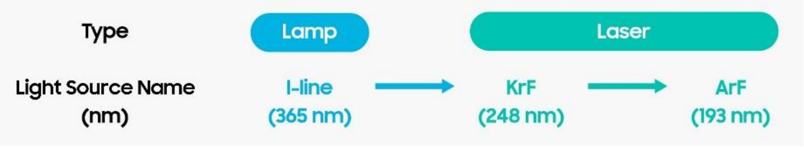
건식 현상 공정 – 쓰러짐의 최소화



Dry resist process flow: Precursor canister delivery, dry deposition, EUV exposure, and dry develop.

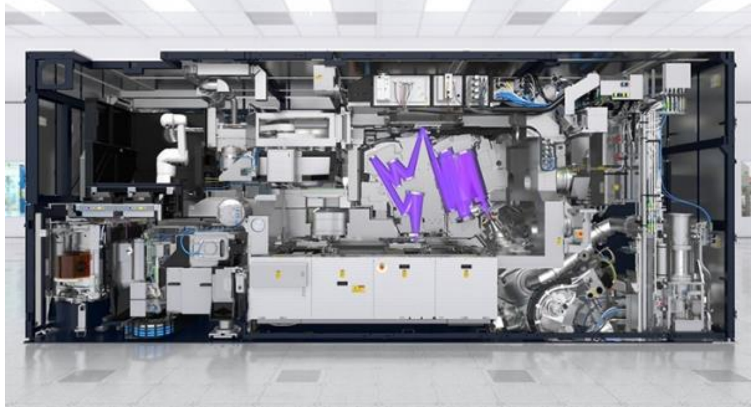
반도체 I Unit Process - Litho

공정	노광 (Photo-Litho)
회사	ASML
기술	KrF, ArF, EUV (파장), 분해능

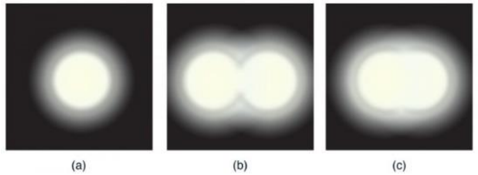


Type	Lamp		Laser		
Light Source Name (nm)	I-line (365 nm)	→	KrF (248 nm)	→	ArF (193 nm)

EUV 설비



분해능 (Resolution)



Bragg's Law : $2d\sin\theta = n\lambda$

$$\Rightarrow 2d = n\lambda/\sin\theta$$

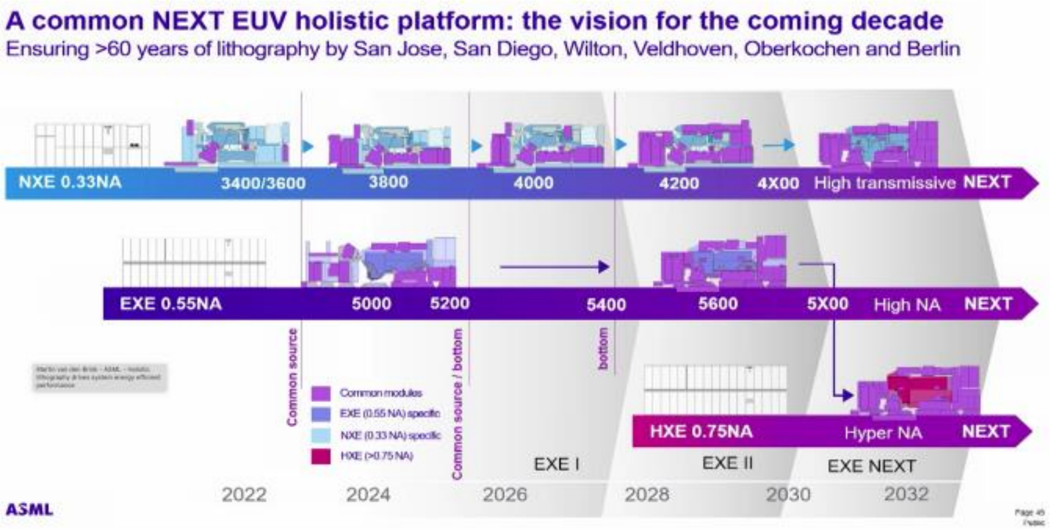
$$\text{Resolution} = K\frac{\lambda}{NA}$$

K : Process Constant
NA : Numerical aperture

반도체 I Unit Process - Litho

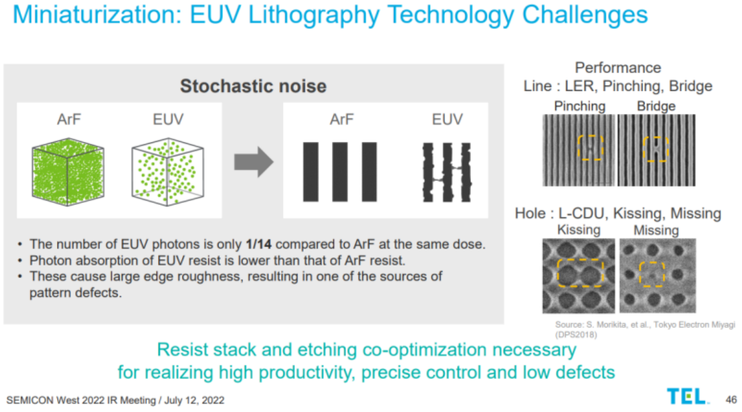
공정	노광 (Photo-Litho)
회사	ASML
기술	KrF, ArF, EUV (파장), 분해능

High NA



A common NEXT EUV holistic platform: the vision for the coming decade

Ensuring >60 years of lithography by San Jose, San Diego, Wilton, Veldhoven, Oberkochen and Berlin



Miniaturization: EUV Lithography Technology Challenges

- The number of EUV photons is only **1/14** compared to ArF at the same dose.
- Photon absorption of EUV resist is lower than that of ArF resist.
- These cause large edge roughness, resulting in one of the sources of pattern defects.

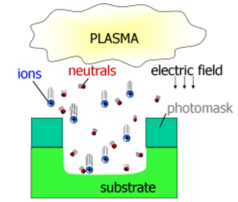
Source: S. Morikita, et al., Tokyo Electron Miyagi (DPS2018)

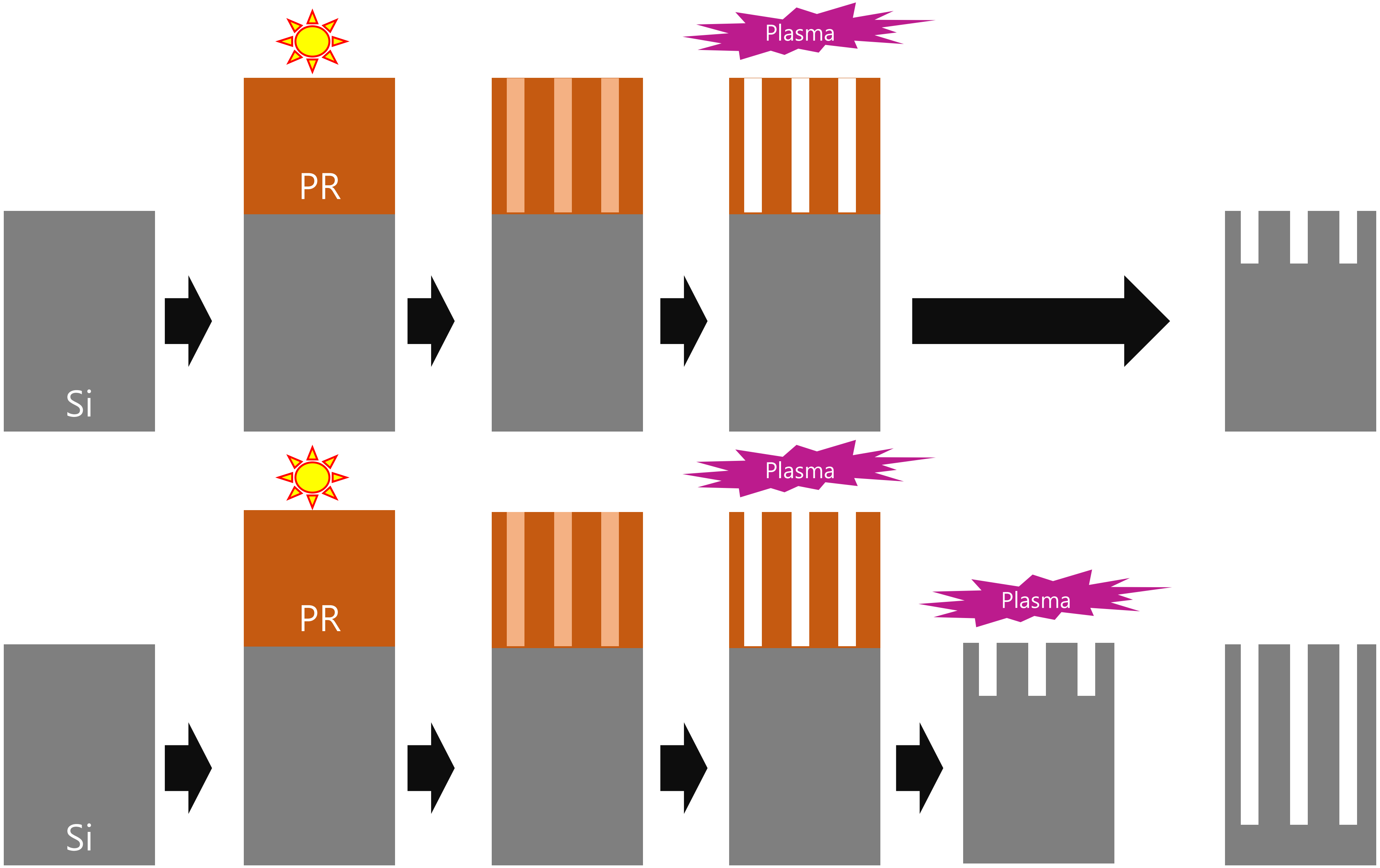
Resist stack and etching co-optimization necessary
for realizing high productivity, precise control and low defects

SEMICON West 2022 IR Meeting / July 12, 2022

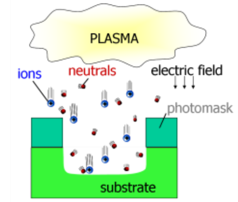
TEL 46

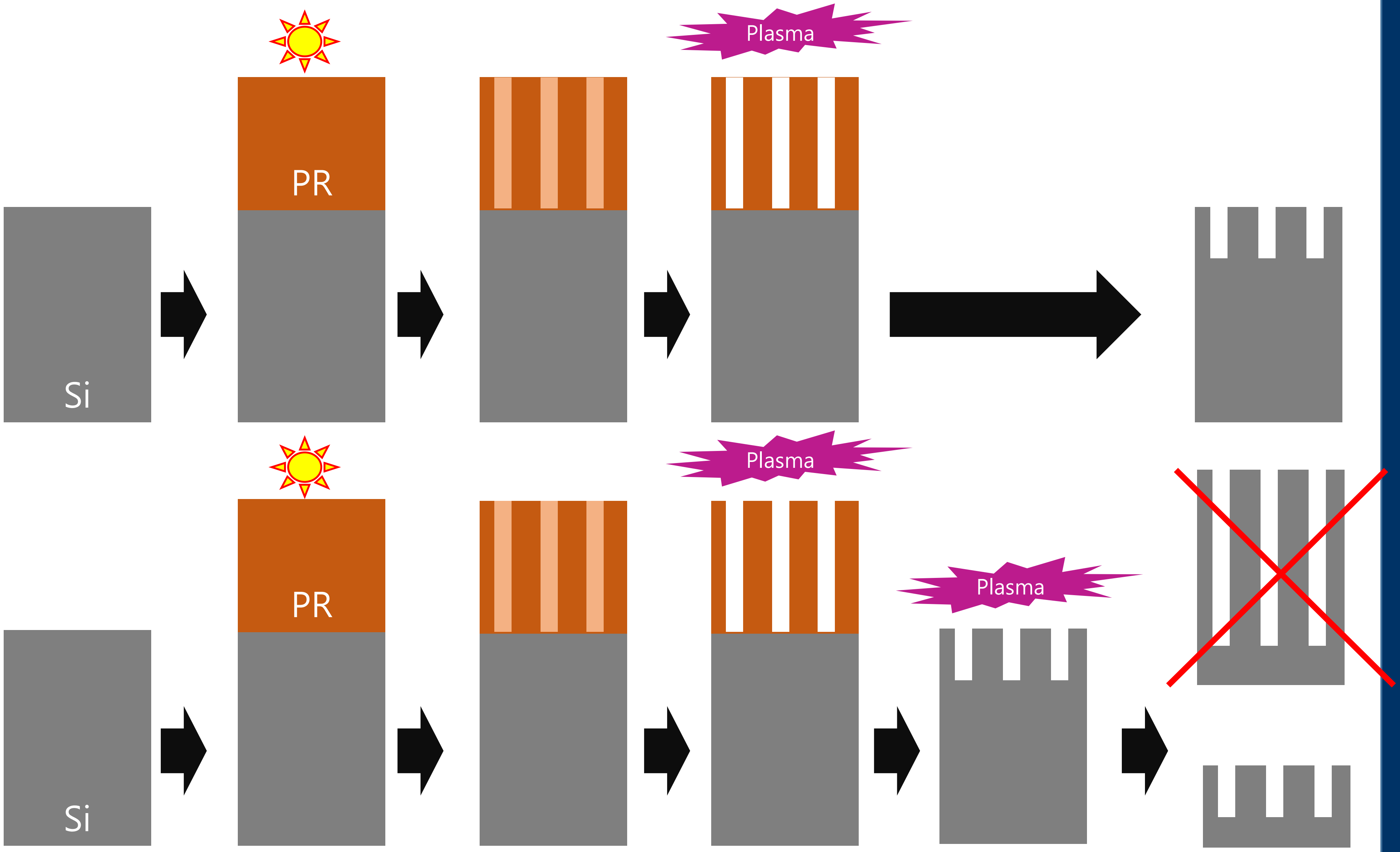
반도체 | Unit Process - Etch

공정	**식각 (Etch)**
회사	Lam Research APPLIED MATERIALS TEL
기술	Plasma Etch, ALE, Selective Etch
	

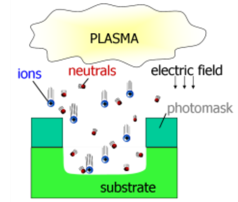


반도체 | Unit Process - Etch

공정	**식각 (Etch)**
회사	Lam Research APPLIED MATERIALS TEL
기술	Plasma Etch, ALE, Selective Etch
	

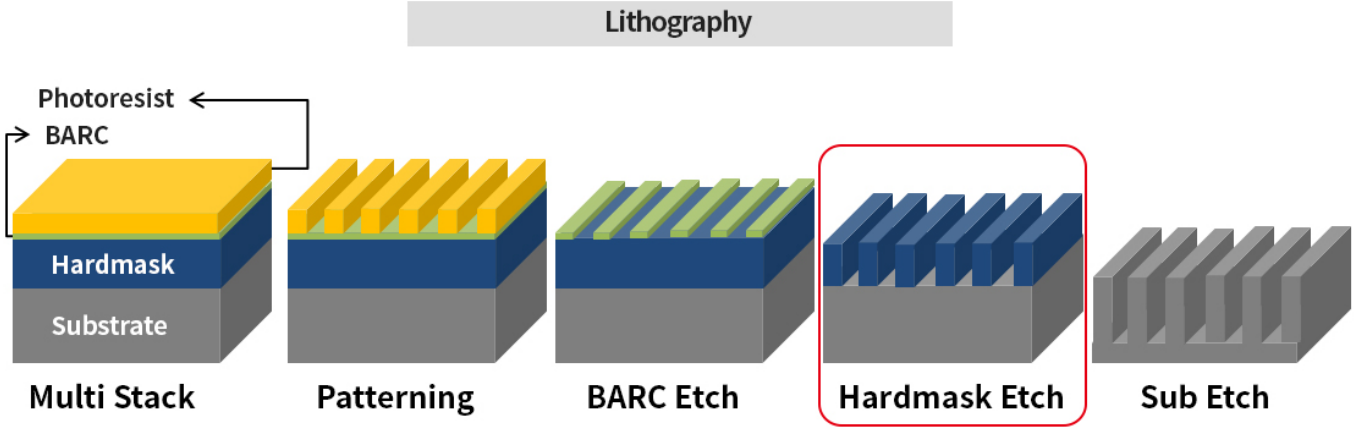


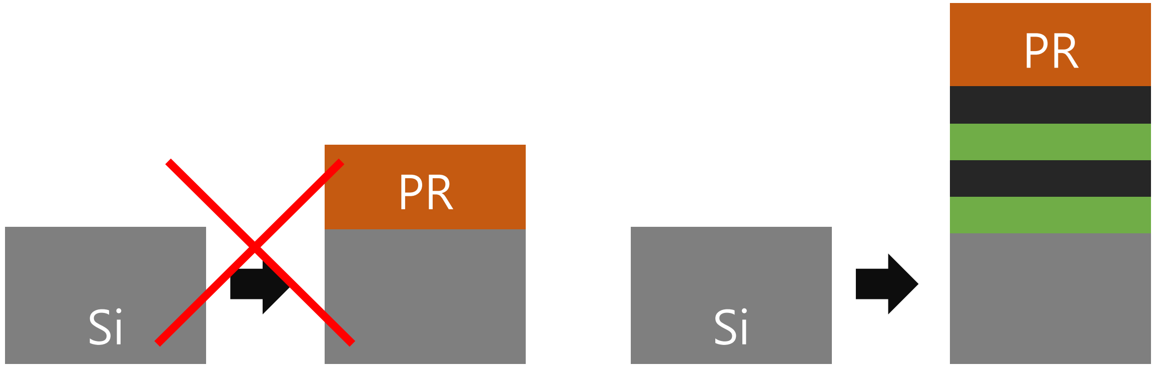
반도체 | Unit Process - Etch

공정	식각 (Etch)
회사	Lam RESEARCH APPLIED MATERIALS TEL
기술	Plasma Etch, ALE, Selective Etch
	

하드마스크 (Spin-on-carbon (SOC) Hardmask)

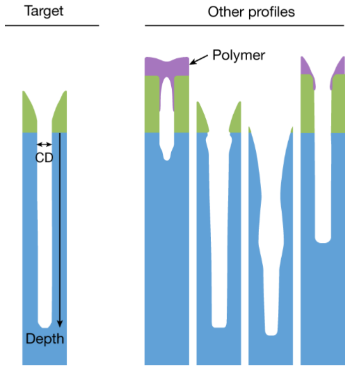
미세회로 형성을 위해 Photoresist Film의 두께가 얇아짐에 따라 Etch 공정에서 Photoresist만으로 Mask 역할의 수행이 어려워, Etch Masking 재료로서 도입된 물질로 차세대 반도체 제조에 필수적인 재료입니다.





Carbon-based (ACL)

Si-based (SiON)

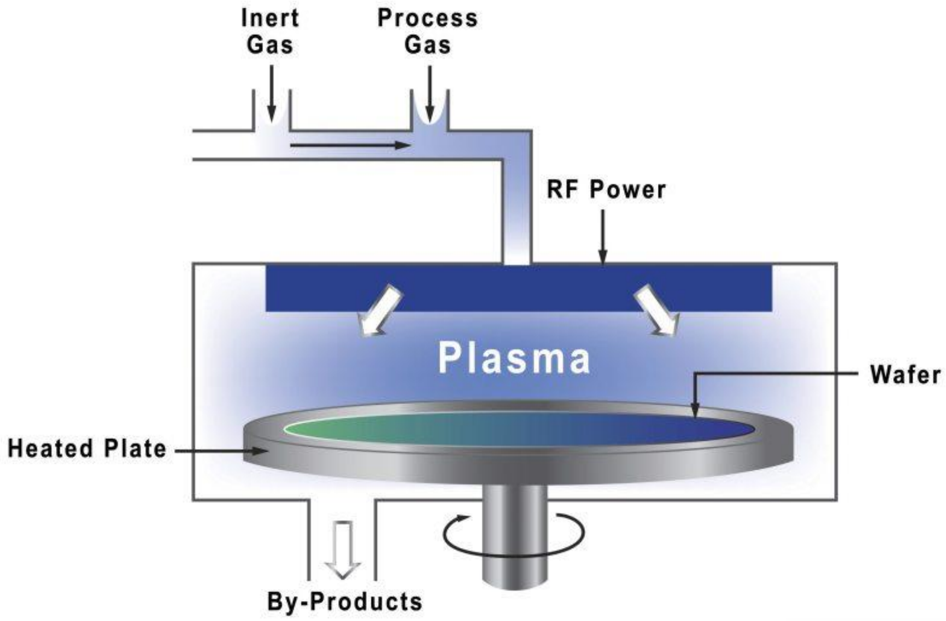


반도체 I Unit Process - Depo

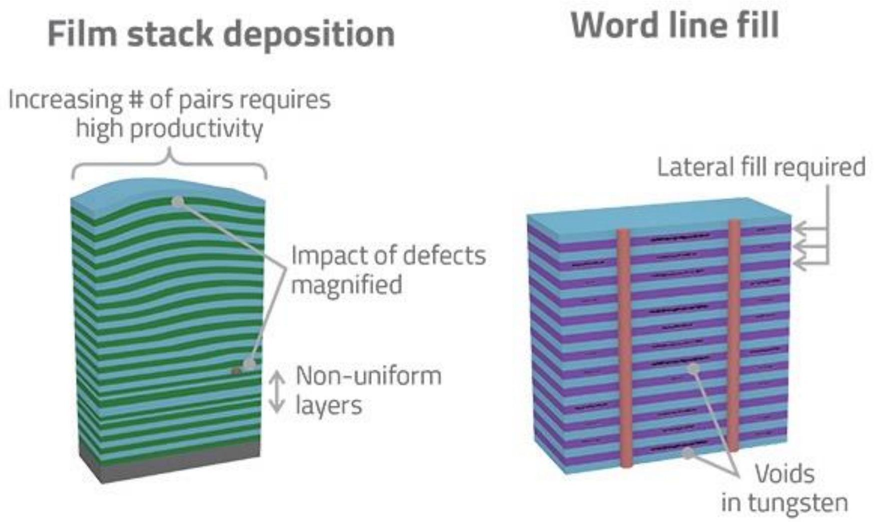
공정	증착 (Depo)
회사	APPLIED MATERIALS
기술	CVD, PECVD, ALD

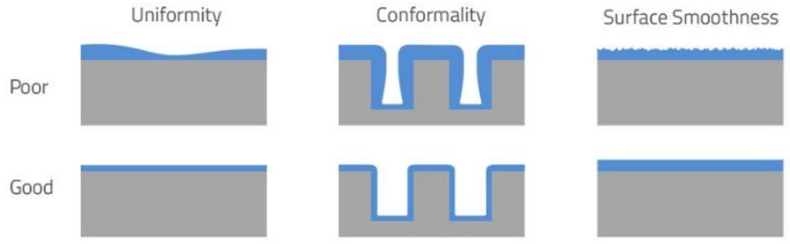
PECVD

(Plasma Enhanced Chemical Vapor Deposition)

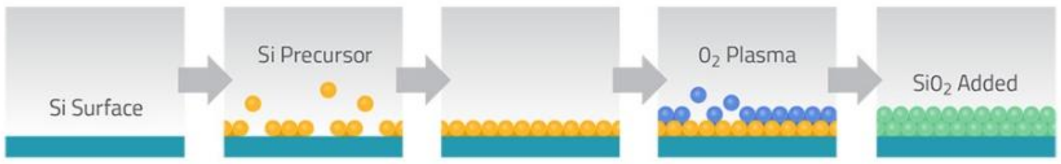


Dielectric or Metal





ALD Process (SiO_2 Example)



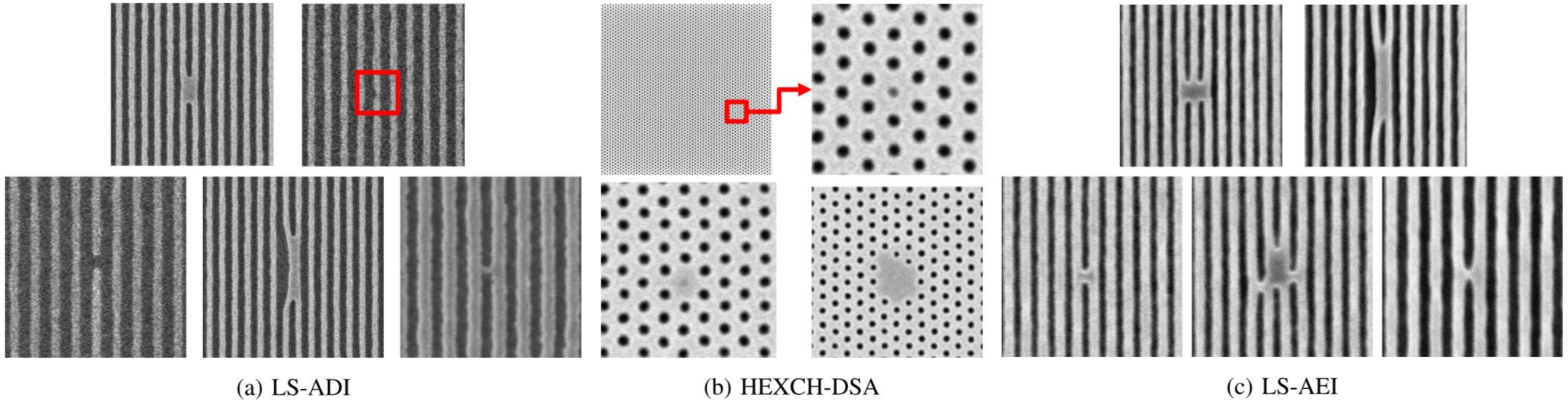
반도체 I Unit Process - 검사

Metrology & Inspection

공정	검사
회사	KLA APPLIED MATERIALS HITACHI Inspire the Next
기술	광학, E-beam

Defect 찾기 (Inspection)

DOI: 10.1109/ELMAR62909.2024.10694600

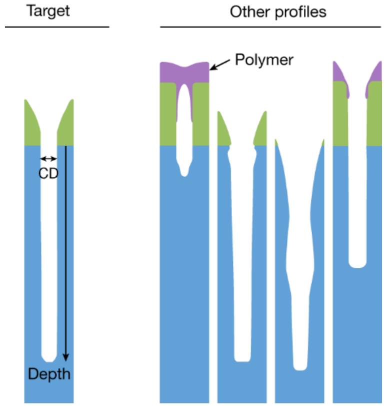


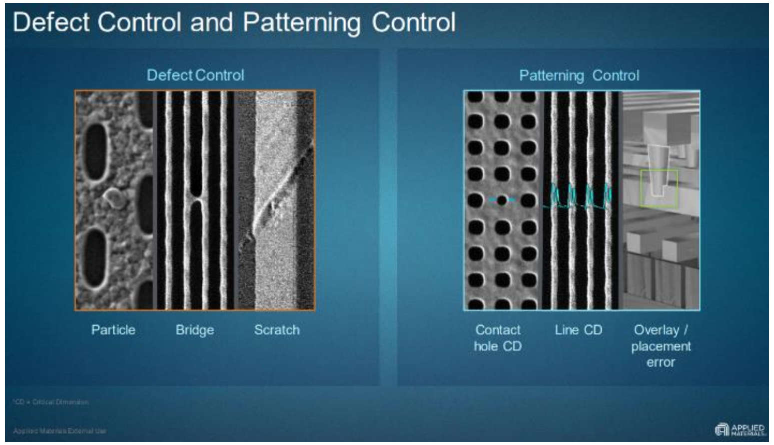
(a) LS-ADI

(b) HEXCH-DSA

(c) LS-AEI

계측 (Metrology) : CD, Depth, Thickness, OVL etc..

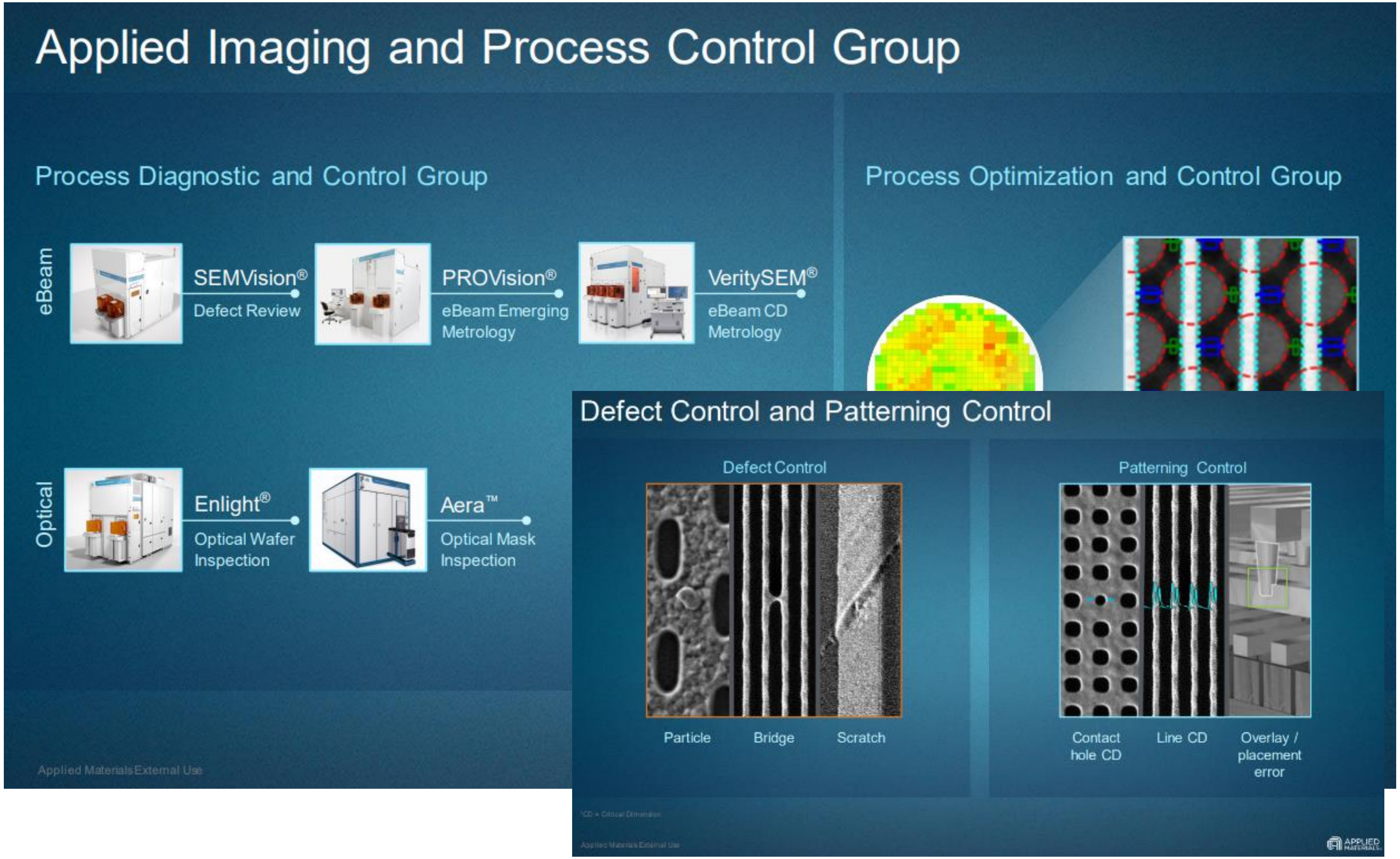



Defect Control and Patterning Control

반도체 | Unit Process - 검사

Metrology & Inspection

공정	검사
회사	APPLIED MATERIALS KLA HITACHI Inspire the Next
기술	광학, E-beam



Applied Imaging and Process Control Group

Process Diagnostic and Control Group

Process Optimization and Control Group

eBeam

SEMVision® Defect Review

PROVision® eBeam Emerging Metrology

VeritySEM® eBeam CD Metrology

Optical

Enlight® Optical Wafer Inspection

Aera™ Optical Mask Inspection

Applied Materials External Use

Defect Control and Patterning Control

Defect Control

Particle

Bridge

Scratch

Patterning Control

Contact hole CD

Line CD

Overlay / placement error

*CD = Critical Dimension

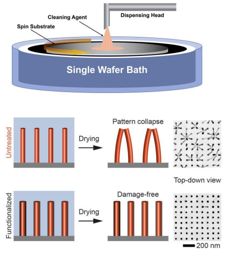
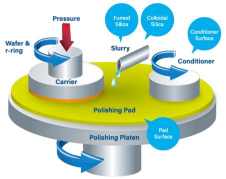
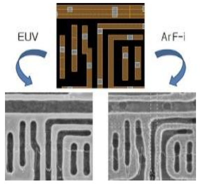
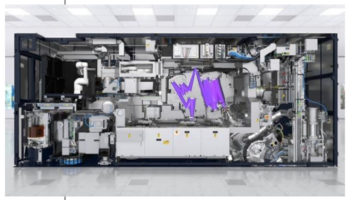
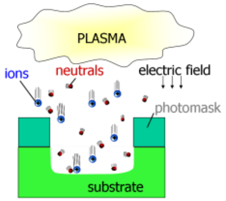
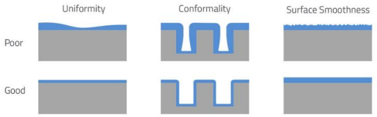
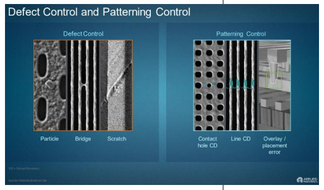
Applied Materials External Use

Intro I 반도체 Workflow

Device & Process Design → Unit Process → 수율 및 불량 분석 → Packaging

8대 공정 : Clean, CMP, Photo (Litho), Etch, Depo, Inspection & Metrology

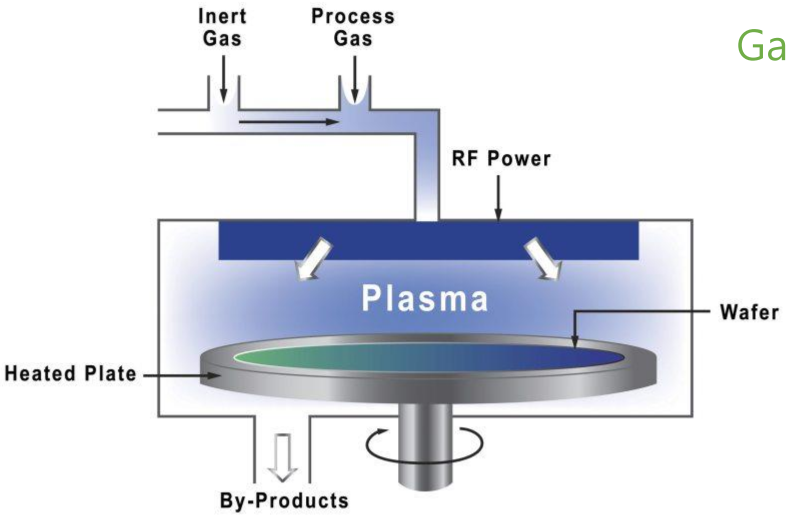
준비 → 패턴 → 증착 → 검사

공정	세정 (Wet Clean)	평탄화 (CMP)	PR 도포/현상 (Spinner)	노광 (Photo-Litho)	식각 (Etch)	증착 (Depo)	검사
회사	SCREEN TEL	APPLIED MATERIALS	TEL	ASML	Lam RESEARCH APPLIED MATERIALS TEL	APPLIED MATERIALS	KLA APPLIED MATERIALS HITACHI Inspire the Next
기술	나노 파티클 제거, 초임계, 공학 (로봇 등)	Slurry, Warpage	Spin 코팅, 현상, 공학 (로봇 등)	KrF, ArF, EUV (파장), 분해능	Plasma Etch, ALE, Selective Etch	CVD, PECVD, ALD	광학, E-beam
							

마치며...

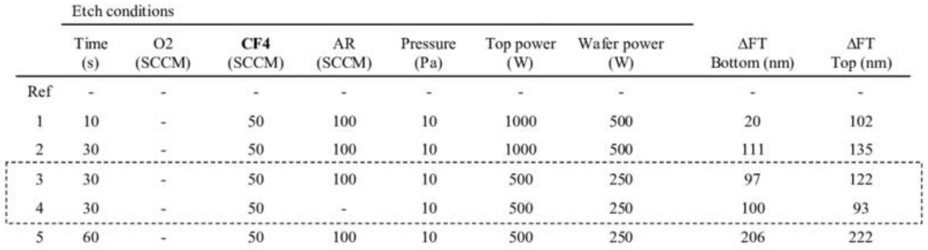
Device & Process Design → **Unit Process** → **수율 및 불량 분석** → **Packaging**

8대 공정 : Clean, CMP, Photo (Litho), Etch, Depo, Inspection & Metrology

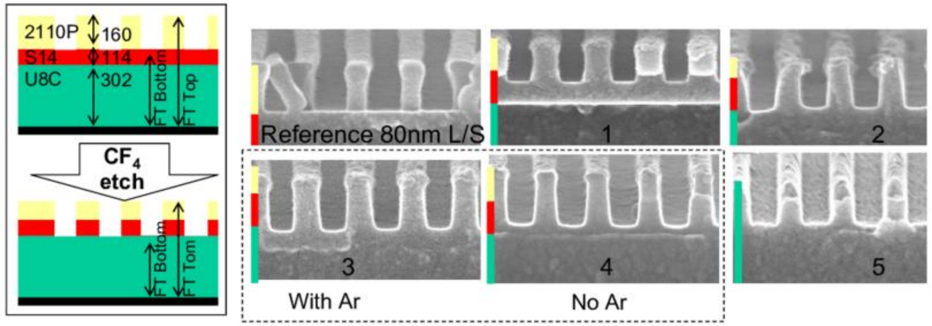


Gas1 flow, Gas2 flow, Gas Ratio, Pressure, RF Power, Temperature, Time etc..

→ **Design of Experiment (DOE)**



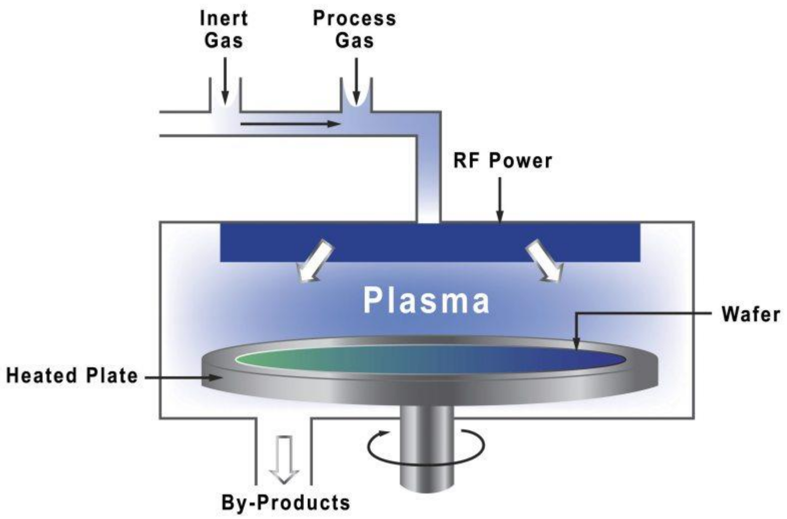
	Etch conditions								
	Time (s)	O2 (SCCM)	**CF4** (SCCM)	AR (SCCM)	Pressure (Pa)	Top power (W)	Wafer power (W)	ΔFT Bottom (nm)	ΔFT Top (nm)
Ref	-	-	-	-	-	-	-	-	-
1	10	-	50	100	10	1000	500	20	102
2	30	-	50	100	10	1000	500	111	135
3	30	-	50	100	10	500	250	97	122
4	30	-	50	-	10	500	250	100	93
5	60	-	50	100	10	500	250	206	222



마치며...

Device & Process Design → Unit Process → 수율 및 불량 분석 → Packaging

8대 공정 : Clean, CMP, Photo (Litho), Etch, Depo, Inspection & Metrology



기술적 깊이 및 실험 DOE에 대한 이해

공정 측면
Etch – Hard mask 용도 (선택비), Parameter별 따른 특성, Gas ratio에 따른 현상 등

Dep – Conformity를 위해 뭘 해야 하는지, 또한 어떤 실험들을 했는지 등

H/W 측면 : 왜 그런 부품들을 사용하는지

얼마나 끈길기게 사고하고 집중하고 실험 하는지...

감사합니다.

Appendix